

TC74HC646AP

Octal Bus Transceiver/Register (3-state)

The TC74HC646A is high speed CMOS OCTAL BUS TRANSCEIVER/REGISTERS fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device is bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

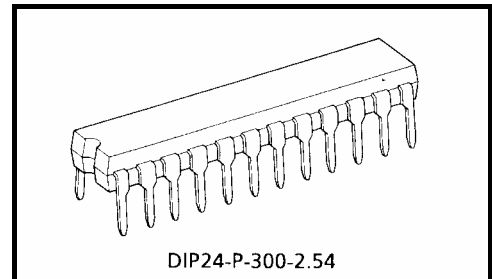
When the direction input (DIR) is held high, the A1 thru A8 become inputs and the B1 thru B8 become outputs. When the DIR input is held low, the A1 thru A8 become output and the B1 thru B8 become inputs.

The enable input \overline{G} is held high, both the A Bus and B Bus become high impedance.

The select inputs (SAB, SBA) can multiplex stored and real-time (transparent mode) data.

Data on the A Bus or B Bus can be clocked into the registers on the positive going transition of either CAB or CBA clock inputs, respectively.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Weight: 1.50 g (typ.)

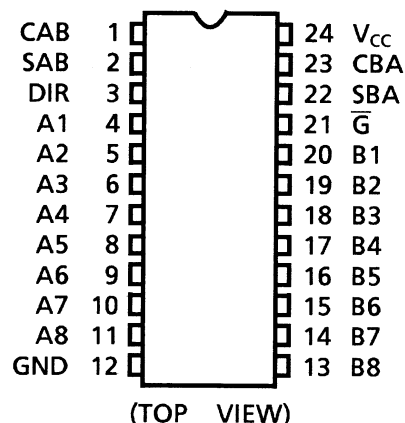
Features (Note 1) (Note 2)

- High speed: $f_{max} = 73$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 4 \mu A$ (max) at $T_a = 25^\circ C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Output drive capability: 15 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 6$ mA (min)
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC} (opr) = 2$ to 6 V
- Pin and function compatible with 74LS646

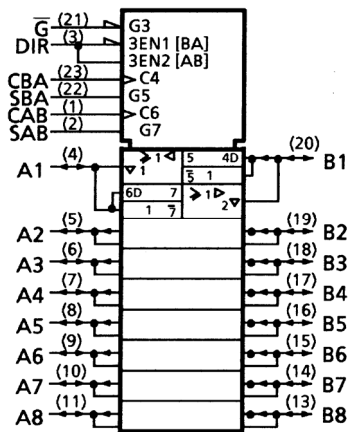
Note 1: Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.

Note 2: All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

Pin Assignment



IEC Logic Symbol



Truth Table

\bar{G}	DIR	CAB	CBA	SAB	SBA	A	B	Function
H	X	X (Note)	X (Note)	X	X	Inputs Z	Inputs Z	The output functions of A and B busses are disabled.
				X	X	X	X	Both A and B busses are used as inputs to the internal flip-flops. Data on the bus will be stored on the rising edge of the clock.
L	H	X	X (Note)	L	X	Inputs L H	Outputs L H	The data on the A bus are displayed on the B bus.
			X (Note)	L	X	L H	L H	The data on the A bus are displayed on the B bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X	X (Note)	H	X	X	Qn	The data in the A storage flip-flops are displayed on the B bus.
			X (Note)	H	X	L H	L H	The data on the A bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B bus.
L	L	X (Note)	X (Note)	X	L	Outputs L H	Inputs L H	The data on the B bus are displayed on the A bus.
		X (Note)		X	L	L H	L H	The data on the B bus are displayed on the A bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X (Note)	X (Note)	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A bus.
		X (Note)		X	H	L H	L H	The data on the B bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A bus.

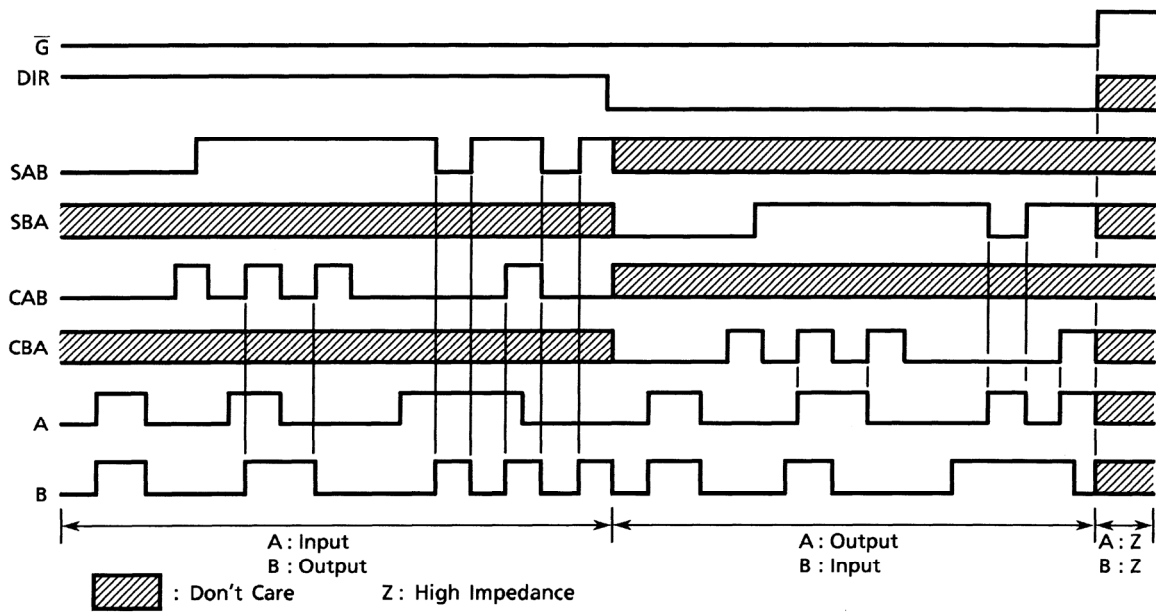
X: Don't care

Qn: The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.

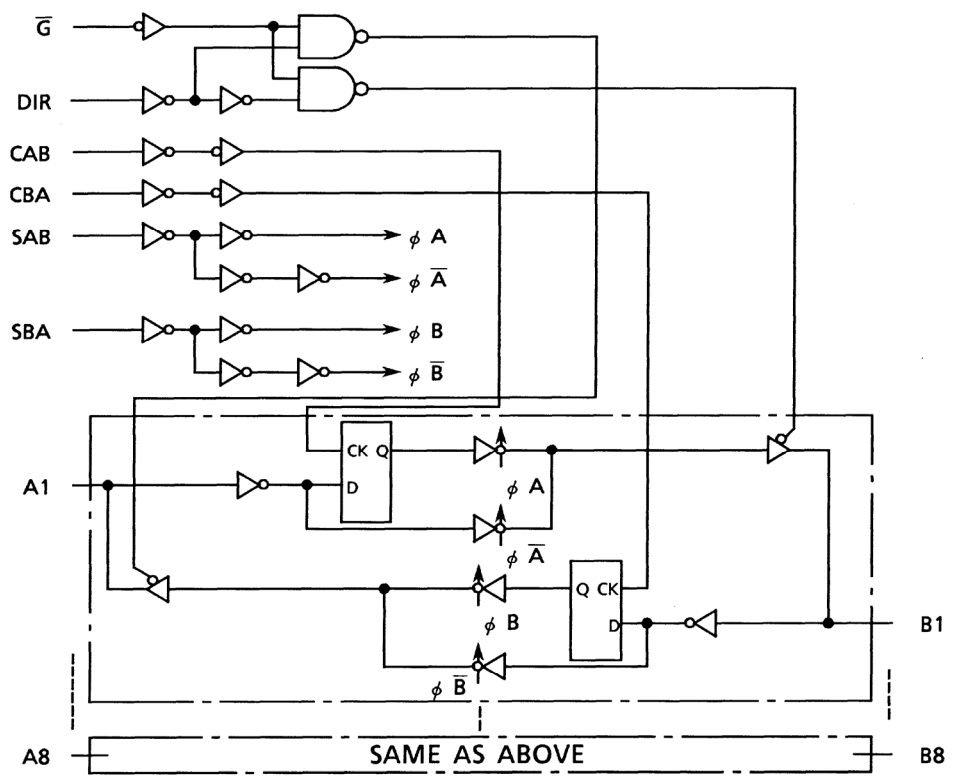
Z: High impedance

Note: The clocks are not internally gated with either \bar{G} or DIR. Therefore, data on the A and/or B busses may be clocked into the storage flip-flops at any time.

Timing Chart



System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 35	mA
DC V_{CC} /ground current	I_{CC}	± 75	mA
Power dissipation	P_D	500 (Note 2)	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of -10 mW/°C shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 ($V_{CC} = 2.0$ V) 0 to 500 ($V_{CC} = 4.5$ V) 0 to 400 ($V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V _{CC} (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V _{IH}	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V _{IL}	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I _{OH} = -6 mA	4.5	4.18	4.31	—	4.13	—	
				6.0	5.68	5.80	—	5.63	—	
				I _{OH} = -7.8 mA	4.5	—	—	—	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			I _{OL} = 6 mA	4.5	—	0.17	0.26	—	0.33	
				6.0	—	0.18	0.26	—	0.33	
				I _{OL} = 7.8 mA	4.5	—	—	—	—	
3-state output off-state current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	6.0	—	—	±0.5	—	±5.0	μA	
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND	6.0	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND	6.0	—	—	4.0	—	40.0	μA	

Timing Requirements (input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C	Unit	
				V _{CC} (V)	Typ.	Limit		Limit
Minimum pulse width (CK)	t _W (H) t _W (L)	—		2.0	—	75	95	ns
				4.5	—	15	19	
				6.0	—	13	16	
Minimum set-up time	t _s	—		2.0	—	50	65	ns
				4.5	—	10	13	
				6.0	—	9	11	
Minimum hold time	t _h	—		2.0	—	5	5	ns
				4.5	—	5	5	
				6.0	—	5	5	
Clock frequency	f	—		2.0	—	6	5	MHz
				4.5	—	31	25	
				6.0	—	36	29	

AC Characteristics (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit			
			CL (pF)	VCC (V)	Min	Typ.	Max		Min	Max	
Output transition time	t_{TLH} t_{THL}	—	50	2.0	—	25	60	—	75	ns	
				4.5	—	7	12	—	15		
Propagation delay time (BUS-bus)	t_{pLH} t_{pHL}	—	50	2.0	—	74	150	—	190	ns	
				4.5	—	21	30	—	38		
			150	2.0	—	91	190	—	240		ns
				4.5	—	26	38	—	48		
Propagation delay time (CAB, CBA-bus)	t_{pLH} t_{pHL}	—	50	2.0	—	98	210	—	265	ns	
				4.5	—	28	42	—	53		
			150	2.0	—	116	250	—	315		ns
				4.5	—	33	50	—	63		
Propagation delay time (SAB, SBA-bus)	t_{pLH} t_{pHL}	—	50	2.0	—	81	170	—	215	ns	
				4.5	—	23	34	—	43		
			150	2.0	—	98	210	—	265		ns
				4.5	—	28	42	—	53		
Output enable time (\bar{G} , DIR-bus)	t_{pZL} t_{pZH}	$R_L = 1$ k Ω	50	2.0	—	84	175	—	220	ns	
				4.5	—	24	35	—	44		
			150	2.0	—	102	215	—	270		ns
				4.5	—	29	43	—	54		
Output disable time (\bar{G} , DIR-bus)	t_{pLZ} t_{pHZ}	$R_L = 1$ k Ω	50	2.0	—	60	175	—	220	ns	
				4.5	—	23	35	—	44		
			150	2.0	—	102	215	—	270		ns
				4.5	—	29	43	—	54		
Maximum clock frequency	f_{max}	—	50	2.0	6	19	—	5	—	MHz	
				4.5	31	67	—	25	—		
				6.0	36	79	—	29	—		
Input capacitance	C_{IN}	—	—	—	—	5	10	—	10	pF	
Output capacitance	$C_{I/O}$	—	—	—	—	13	—	—	—	pF	
Power dissipation capacitance	C_{PD} (Note)	—	—	—	—	39	—	—	—	pF	

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

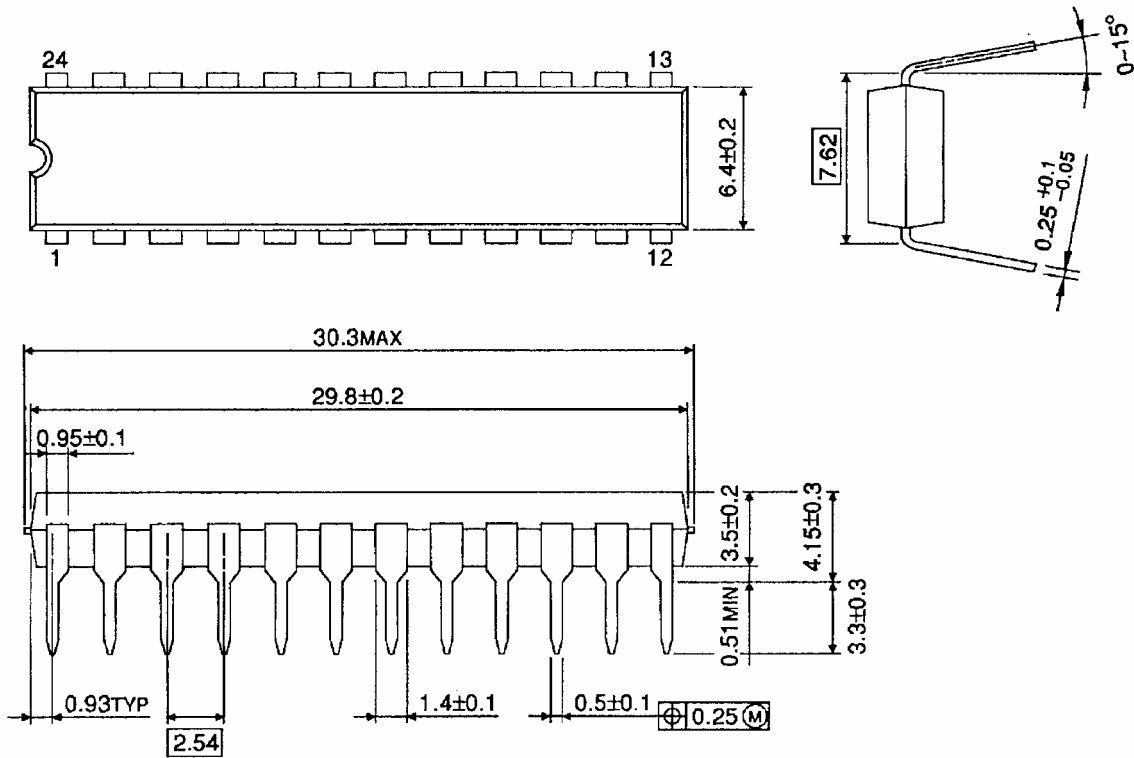
Average operating current can be obtained by the equation:

$$I_{CC} (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

Package Dimensions

DIP24-P-300-2.54

Unit : mm



Weight: 1.50 g (typ.)

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20070701-EN GENERAL

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