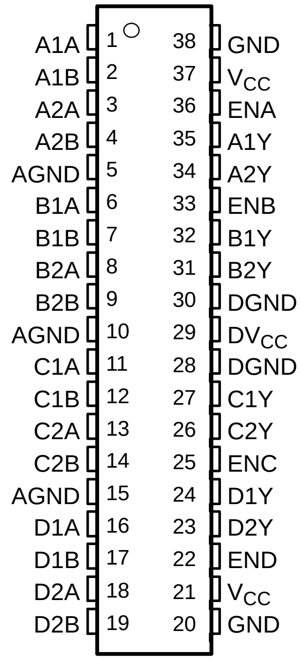
HIGH-SPEED DIFFERENTIAL LINE RECEIVERS

FEATURES

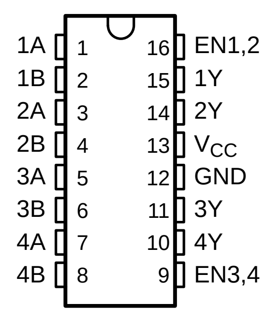
- **Four- ('390), Eight- ('388A), or Sixteen- ('386) Line Receivers Meet or Exceed the Requirements of ANSI TIA/EIA-644 Standard**
- **Integrated 110-Ω Line Termination Resistors on LVDT Products**
- **Designed for Signaling Rates** (1) **Up To 630 Mbps**
- **SN65 Version's Bus-Terminal ESD Exceeds 15 kV**
- **Operates From a Single 3.3-V Supply**
- **Typical Propagation Delay Time of 2.6 ns**
- **Output Skew 100 ps (Typ) Part-To-Part Skew Is Less Than 1 ns**
- **LVTTL Levels Are 5-V Tolerant**
- **Open-Circuit Fail Safe**
- **Flow-Through Pinout**
- **Packaged in Thin Shrink Small-Outline Package With 20-mil Terminal Pitch**

'LVDS388A, 'LVDT388A
DBT PACKAGE
(TOP VIEW)

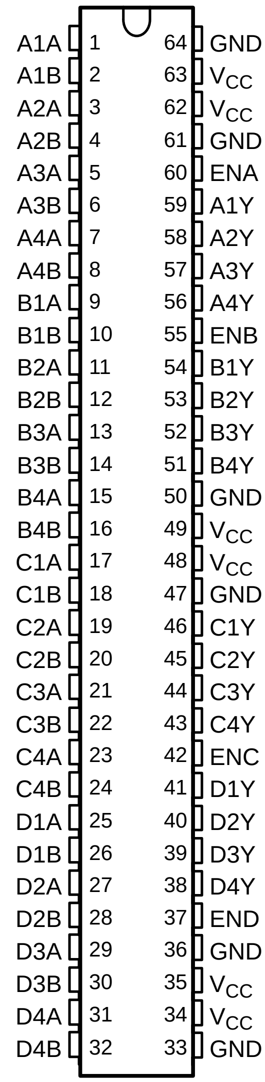


See application section for V_{CC} and GND description.

'LVDS390, 'LVDT390
D OR PW PACKAGE
(TOP VIEW)



'LVDS386, 'LVDT386
DGG PACKAGE
(TOP VIEW)



DESCRIPTION

This family of four-, eight-, or sixteen-, differential line receivers (with optional integrated termination) implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3-V supply rail. Any of the eight or sixteen differential receivers provides a valid logical output state with a ±100-mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes. Additionally, the high-speed switching of LVDS signals almost always requires the use of a line impedance matching resistor at the receiving end of the cable or transmission media. The LVDT products eliminate this external resistor by integrating it with the receiver.

(1) Signaling Rate, 1/t, where t is the minimum unit interval and is expressed in the units bits/s (bits per second)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

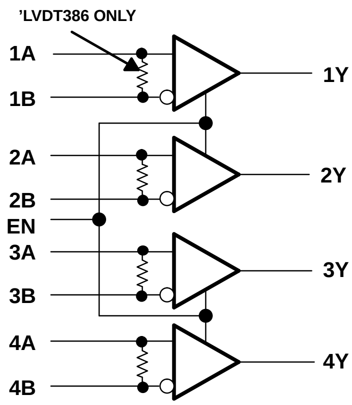
The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of receivers integrated into the same substrate along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. When used with its companion, 8- or 16-channel driver, the SN65LVDS389 or SN65LVDS387, over 300 million data transfers per second in single-edge clocked systems are possible with little power. (Note: The ultimate rate and distance of data transfer depends on the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

AVAILABLE OPTIONS

PART NUMBER	TEMPERATURE RANGE	NUMBER OF RECEIVERS	BUS-PIN ESD	SYMBOLIZATION
SN65LVDS386DGG	–40°C to 85°C	16	15 kV	LVDS386
SN65LVDT386DGG	–40°C to 85°C	16	15 kV	LVDT386
SN75LVDS386DGG	0°C to 70°C	16	4 kV	75LVDS386
SN75LVDT386DGG	0°C to 70°C	16	4 kV	75LVDT386
SN65LVDS388ADBT	–40°C to 85°C	8	15 kV	LVDS388A
SN65LVDT388ADBT	–40°C to 85°C	8	15 kV	LVDT388A
SN75LVDS388ADBT	0°C to 70°C	8	4 kV	75LVDS388A
SN75LVDT388ADBT	0°C to 70°C	8	4 kV	75LVDT388A
SN65LVDS390D	–40°C to 85°C	4	15 kV	LVDS390
SN65LVDS390PW	–40°C to 85°C	4	15 kV	LVDS390
SN65LVDT390D	–40°C to 85°C	4	15 kV	LVDT390
SN65LVDT390PW	–40°C to 85°C	4	15 kV	LVDT390
SN75LVDS390D	0°C to 70°C	4	4 kV	75LVDS390
SN75LVDS390PW	0°C to 70°C	4	4 kV	DS390
SN75LVDT390D	0°C to 70°C	4	4 kV	75LVDT390
SN75LVDT390PW	0°C to 70°C	4	4 kV	DG390

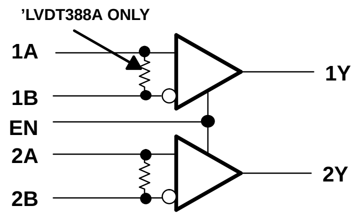
LOGIC DIAGRAM (POSITIVE LOGIC)

’LVDx386



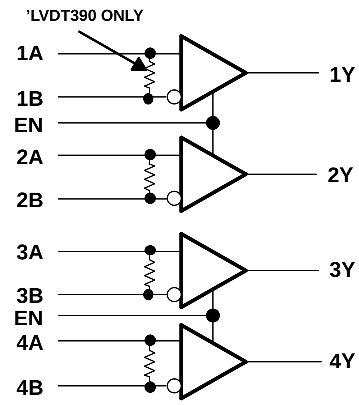
(1/4 of ’LVDx386 shown)

’LVDx388A



(1/4 of ’LVDx388A shown)

’LVDx390



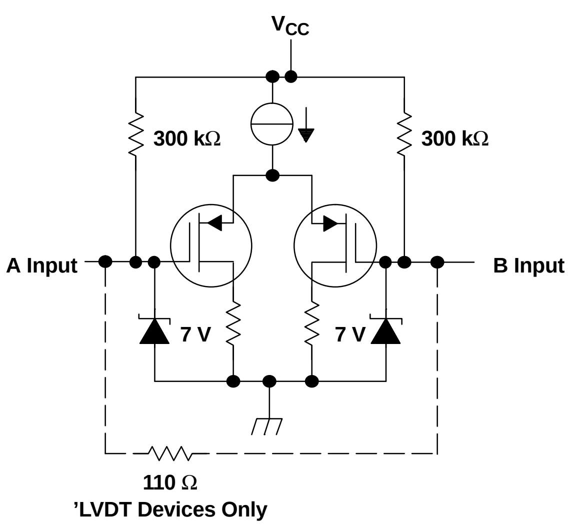
(’LVDx390 shown)

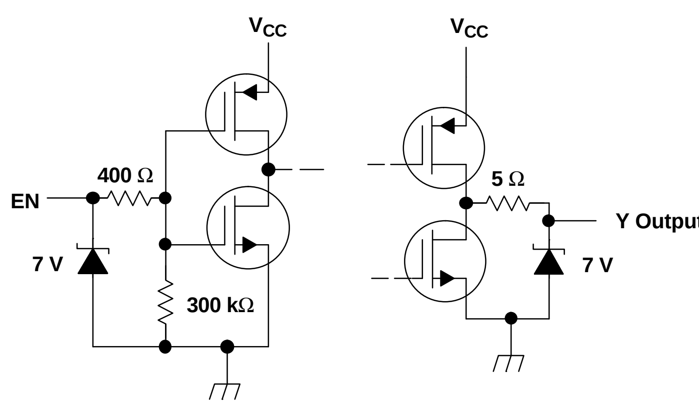
FUNCTION TABLE

SNx5LVD386/388A/390 and SNx5LVDT386/388A/390		
DIFFERENTIAL INPUT(1)	**ENABLES(1)**	**OUTPUT(1)**
A-B	**EN**	**Y**
$V_{ID} \geq$ 100 mV	H	H
–100 mV < $V_{ID} \leq$ 100 mV	H	?
$V_{ID} \leq$ -100 mV	H	L
X	L	Z
Open	H	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS





ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted) (1)

			UNITS
V_{CC} (2)	Supply voltage range		–0.5 V to 4 V
V_I	Voltage range:	Enables or Y	–0.5 V to 6 V
		A or B	–0.5 V to 4 V
I_O	Output current	Y	±12 mA
$\|V_{ID}\|$	Differential input voltage magnitude	SN65LVDT' or SN75LVDT' only	1 V
	Electrostatic discharge: see (3)	SN65' (A, B, and GND)	Class 3, A:15 kV, B: 400 V
		SN75' (A, B, and GND)	Class 2, A:4 kV, B: 400 V
	Continuous power dissipation		See Dissipation Rating Table
T_{stg}	Storage temperature range		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 seconds		260°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR (1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
DBT	1071 mW	8.5 mW/°C	688 mW	556 mW
DGG	2094 mW	16.7 mW/°C	1342 mW	1089 mW
PW	774 mW	6.2 mW/°C	496 mW	402 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) and with no air flow.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_O	Output current	Y	– 8		8	mA
$\|V_{ID}\|$	Magnitude of differential input voltage		0.1		0.6	V
V_{IC}, see Figure 4	Common-mode input voltage		$\frac{\|V_{ID}\|}{2}$		$2.4 - \frac{\|V_{ID}\|}{2}$ $V_{CC} - 0.8$	V
T_A	Operating free-air temperature	SN75'	0		70	°C
		SN65'	–40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold		See Figure 1 and Table 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold			–100			mV
V_{OH}	High-level output voltage		I_{OH} = –8 mA	2.4	3		V
V_{OL}	Low-level output voltage		I_{OL} = 8 mA		0.2	0.4	V
I_{CC}	Supply current	'LVDx386	Enabled, No load		50	70	mA
		'LVDx388A			22	40	
		'LVDx390			8	18	
		'LVDx386	Disabled			3	
		'LVDx388A				3	
		'LVDx390				1.5	
I_I	Input current (A or B inputs)	'LVDS	V_I = 0 V		–13	–20	µA
			V_I = 2.4 V	–1.2	–3		
		'LVDT	V_I = 0 V, other input open			–40	
			V_I = 2.4 V, other input open	–2.4			
I_{ID}	Differential input current $\|I_{IA} - I_{IB}\|$	'LVDS	V_{IA} = 0 V, V_{IB} = 0.1 V, V_{IA}= 2.4 V, V_{IB} = 2.3 V			±2	µA
I_{ID}	Differential input current ($I_{IA} - I_{IB}$)	'LVDT	V_{IA} = 0.2 V, V_{IB} = 0 V, V_{IA}= 2.4 V, V_{IB} = 2.2 V	1.5		2.2	mA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	'LVDS	V_{CC} = 0 V, V_I = 2.4 V		12	±20	µA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	'LVDT	V_{CC} = 0 V, V_I = 2.4 V			±40	µA
I_{IH}	High-level input current (enables)		V_{IH} = 2 V			10	µA
I_{IL}	Low-level input current (enables)		V_{IL} = 0.8 V			10	µA
I_{OZ}	High-impedance output current		V_O = 0 V			±1	µA
			V_O= 3.6 V			10	
C_{IN}	Input capacitance, A or B input to GND		V_{ID} = 0.4 sin 2.5E09 t V		5		pF
$Z_{(t)}$	Termination impedance		V_{ID} = 0.4 sin 2.5E09 t V	88		132	Ω

(1) All typical values are at 25°C and with a 3.3-V supply.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2	1	2.6	4	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1	2.5	4	ns
t_r	Output signal rise time		500	800	1200	ps
t_f	Output signal fall time		500	800	1200	ps
$t_{sk(p)}$	Pulse skew ($\|t_{PHL}$ - $t_{PLH}\|$)			150	600	ps
$t_{sk(o)}$	Output skew[(2)]			100	400	ps
$t_{sk(pp)}$	Part-to-part skew[(3)]				1	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 3		7	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			7	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			7	15	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			7	15	ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of any two devices characterized in this data sheet when both devices operate with the same supply voltage, at the same temperature, and have the same test circuits.

PARAMETER MEASUREMENT INFORMATION

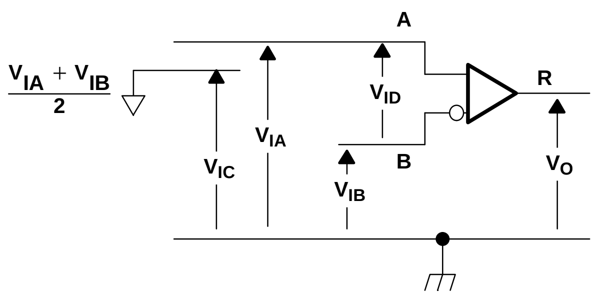
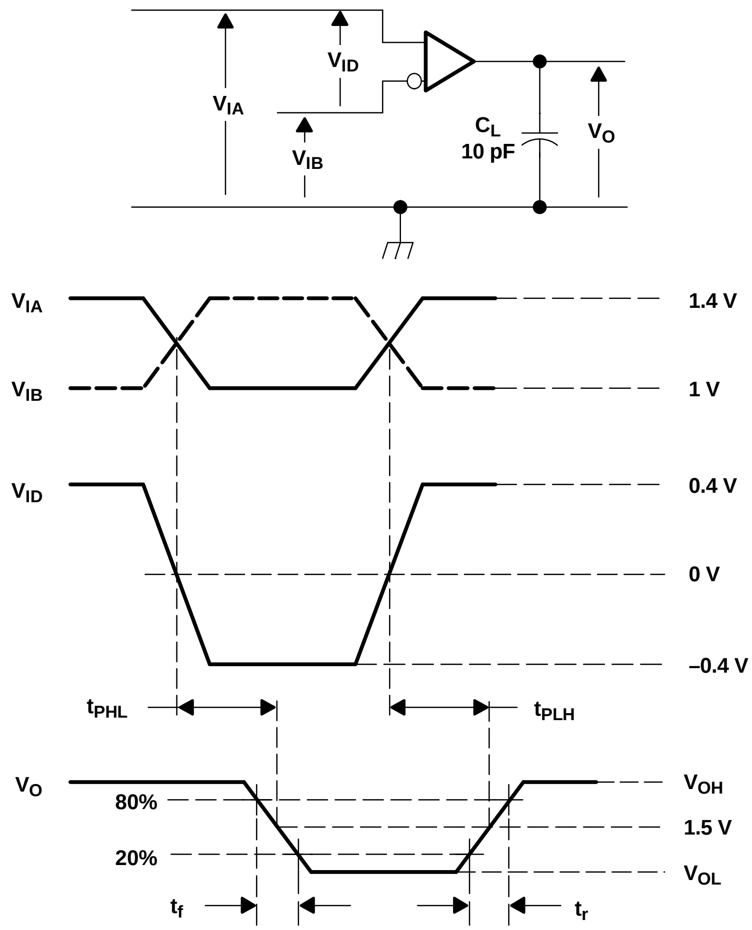


Figure 1. Voltage Definitions

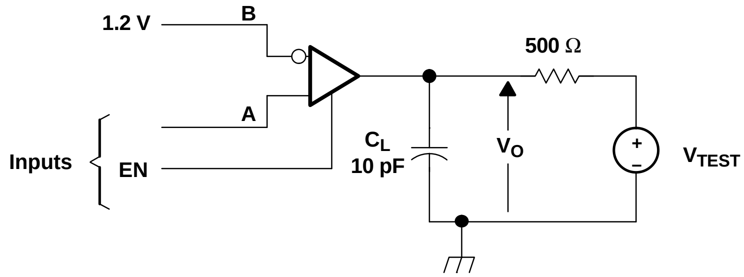
Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	–600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	–600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	–600 mV	0.3 V



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 2. Timing Test Circuit and Wave Forms



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

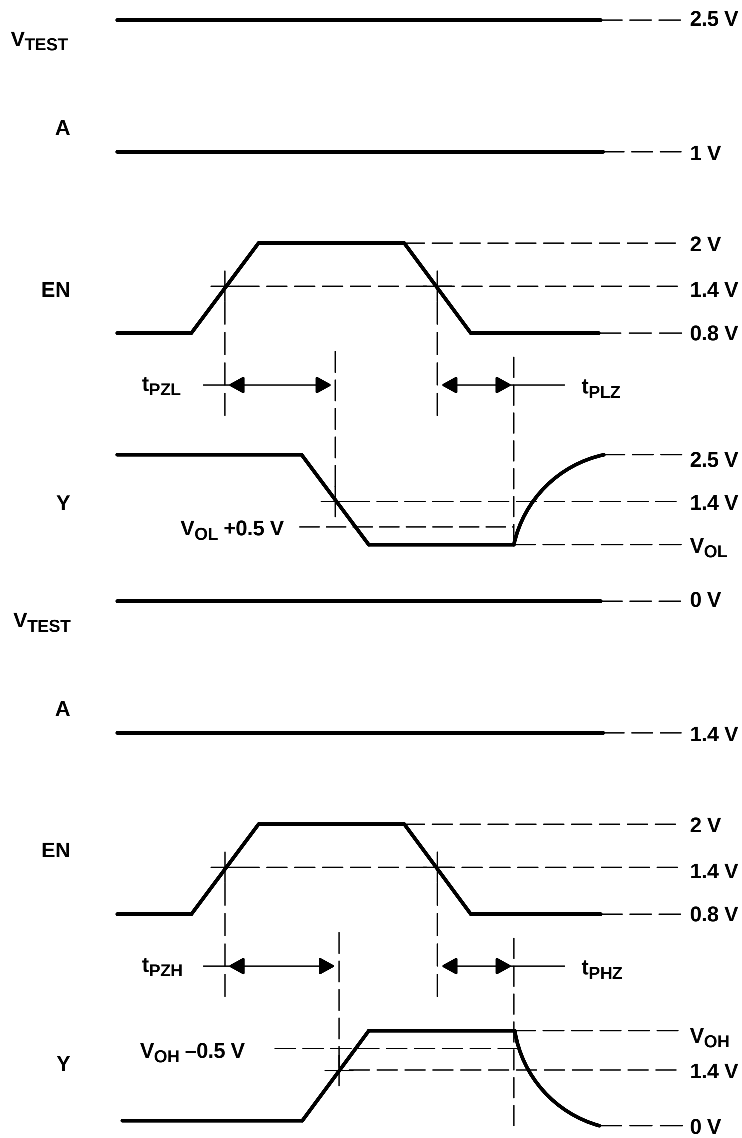


Figure 3. Enable/Disable Time Test Circuit and Wave Forms

TYPICAL CHARACTERISTICS

COMMON-MODE INPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

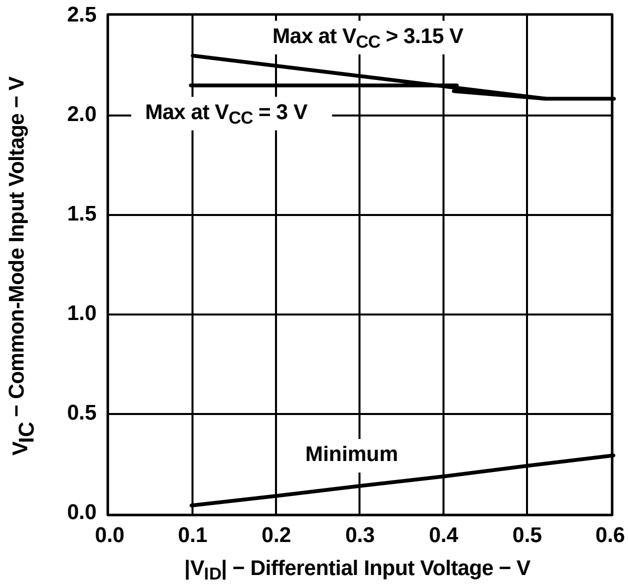


Figure 4.

LVDx390 SUPPLY CURRENT vs SWITCHING FREQUENCY

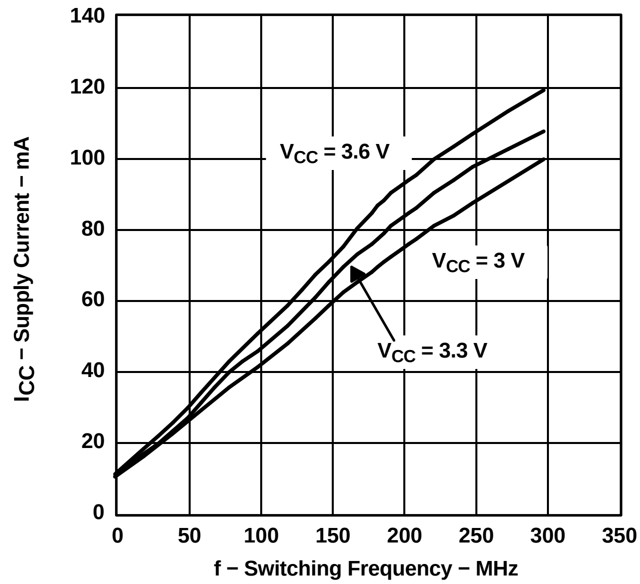


Figure 5.

LVDx388A SUPPLY CURRENT vs SWITCHING FREQUENCY

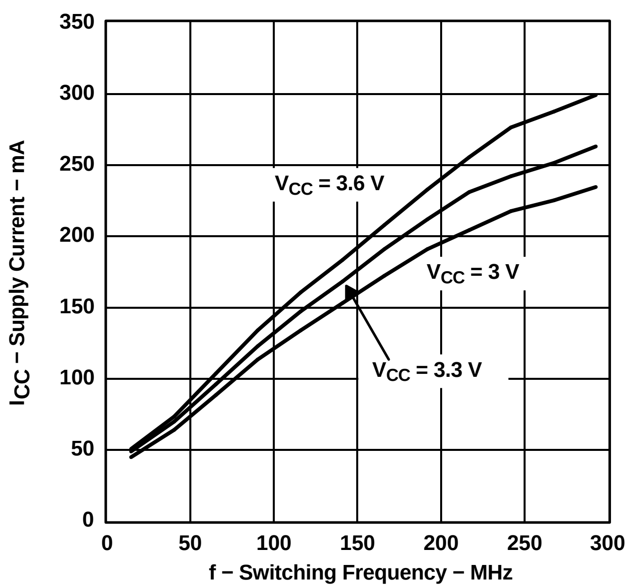


Figure 6.

LVDx386 SUPPLY CURRENT vs SWITCHING FREQUENCY

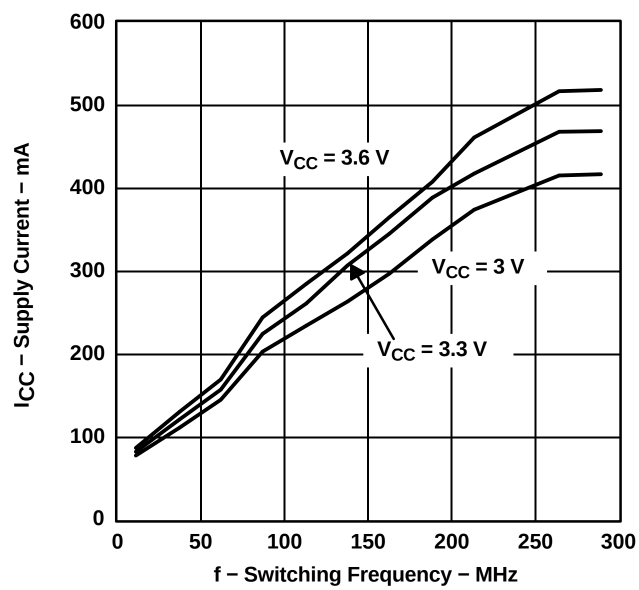


Figure 7.

TYPICAL CHARACTERISTICS (continued)

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

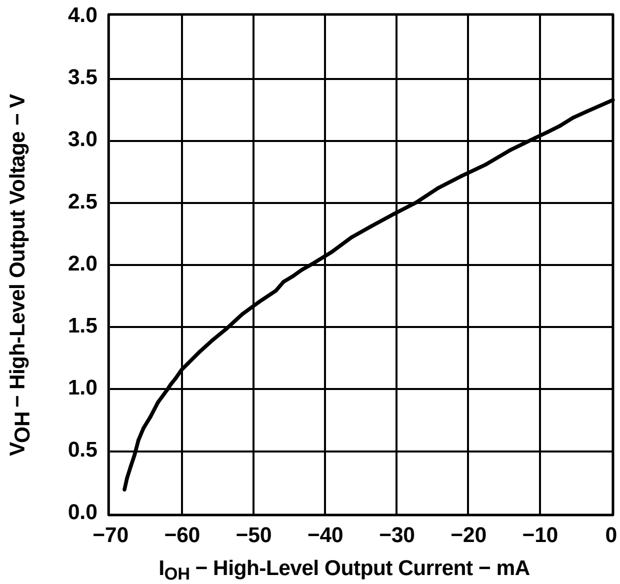


Figure 8.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

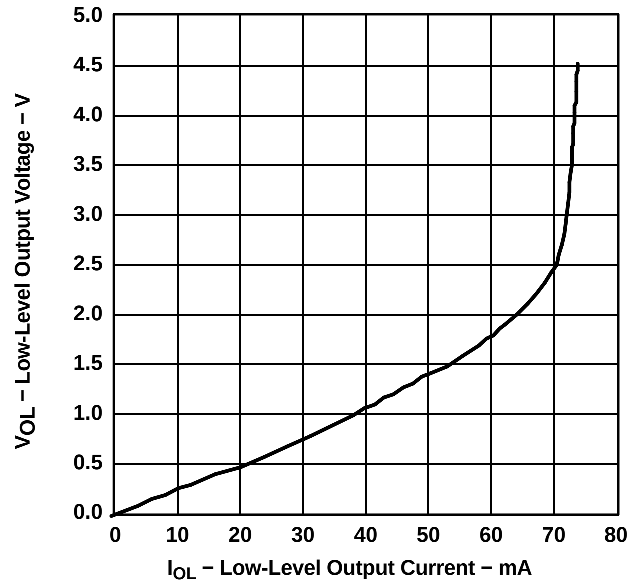


Figure 9.

LOW-TO-HIGH PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

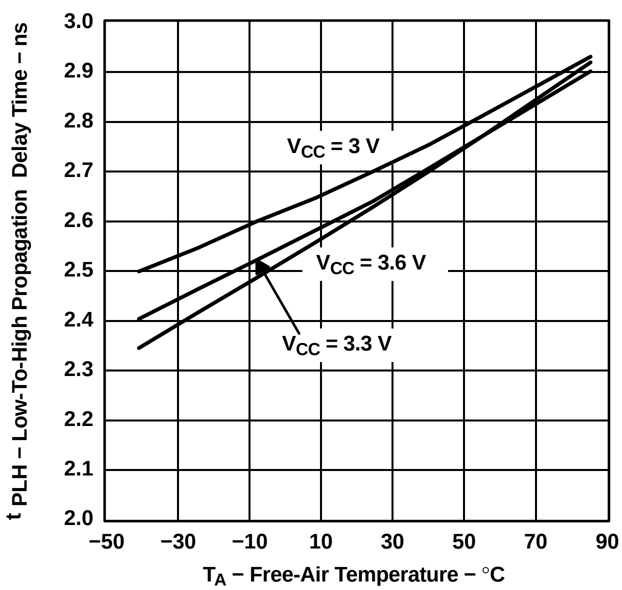


Figure 10.

HIGH-TO-LOW PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

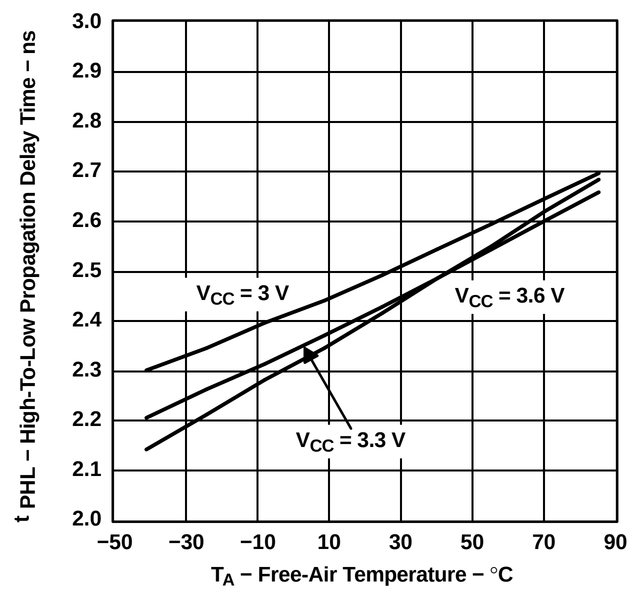


Figure 11.

APPLICATION INFORMATION

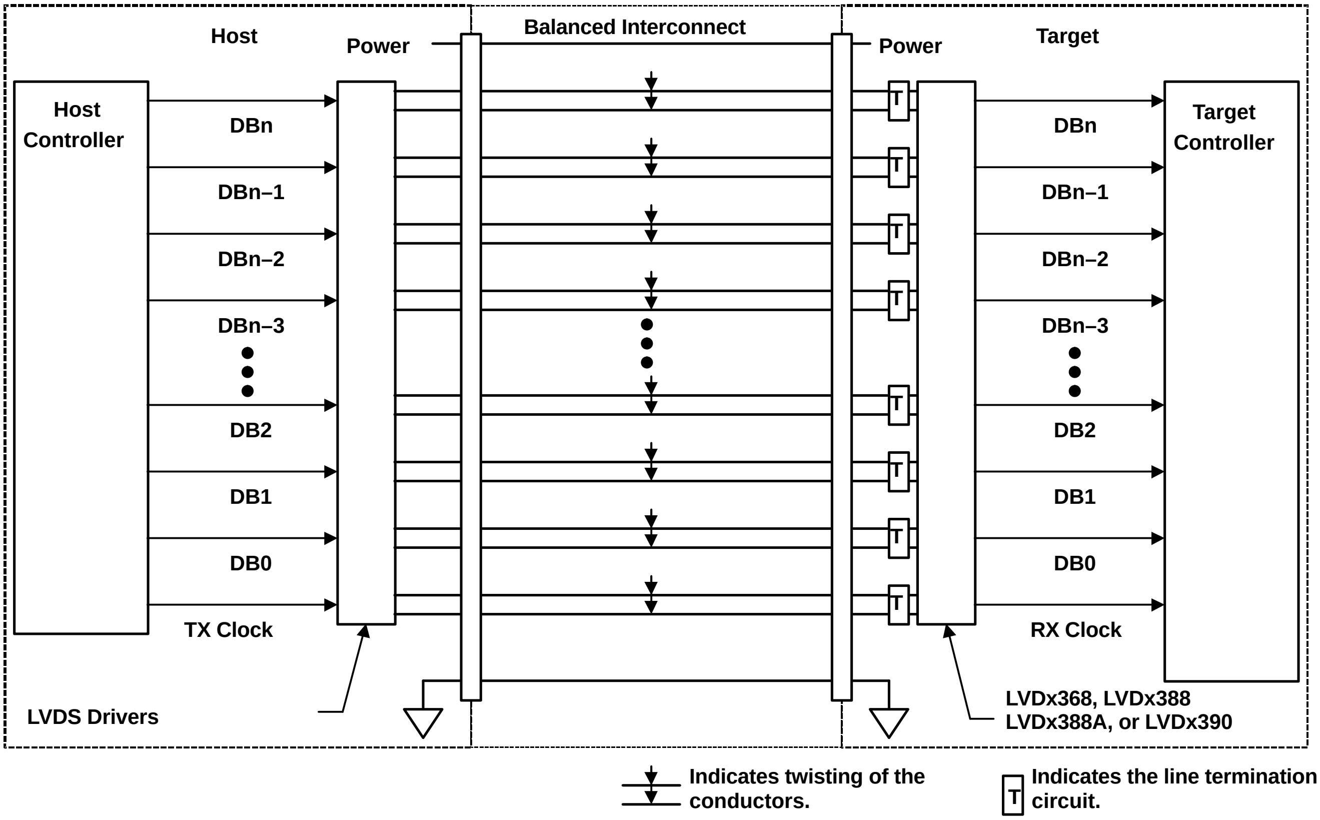


Figure 12. Typical Application Schematic

ANALOG AND DIGITAL GROUNDS/POWER SUPPLIES

Although it is not necessary to separate out the analog/digital supplies and grounds on the SN65LVDS/T388A and SN75LVDS/T388A, the pinout provides the user that option. To help minimize or perhaps eliminate switching noise being coupled between the two supplies, the user could lay out separate supply and ground planes for the designated pinout.

Most applications probably have all grounds connected together and all power supplies connected together. This configuration was used while characterizing and setting the data-sheet parameters.

FAIL SAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV, and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near V_{CC} through 300-kΩ resistors, as shown in Figure 13. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level, regardless of the differential input voltage.

APPLICATION INFORMATION (continued)

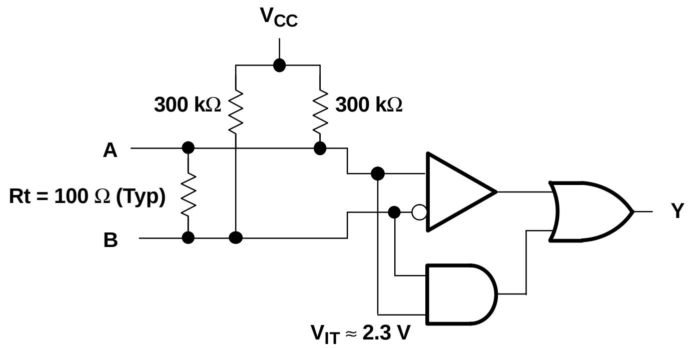


Figure 13. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver is valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN65LVDS386DGG	ACTIVE	TSSOP	DGG	64	25	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS386DGGR	ACTIVE	TSSOP	DGG	64	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS388ADBT	ACTIVE	SM8	DBT	38	50	TBD	CU NIPDAU	Level-2-220C-1 YEAR
SN65LVDS388ADBTR	ACTIVE	SM8	DBT	38	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
SN65LVDS390D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDS390DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDS390PW	ACTIVE	TSSOP	PW	16	90	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS390PWR	ACTIVE	TSSOP	PW	16	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDT386DGG	ACTIVE	TSSOP	DGG	64	25	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDT386DGGG4	PREVIEW	TSSOP	DGG	64	25	TBD	Call TI	Call TI
SN65LVDT386DGGR	ACTIVE	TSSOP	DGG	64	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDT388ADBT	ACTIVE	SM8	DBT	38	50	TBD	CU NIPDAU	Level-2-220C-1 YEAR
SN65LVDT388ADBTR	ACTIVE	SM8	DBT	38	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
SN65LVDT390D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDT390DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDT390PW	ACTIVE	TSSOP	PW	16	90	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDT390PWR	ACTIVE	TSSOP	PW	16	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDS386DGG	ACTIVE	TSSOP	DGG	64	25	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDS386DGGR	ACTIVE	TSSOP	DGG	64	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDS388ADBT	ACTIVE	SM8	DBT	38	50	TBD	CU NIPDAU	Level-2-220C-1 YEAR
SN75LVDS388ADBTR	ACTIVE	SM8	DBT	38	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
SN75LVDS390D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN75LVDS390DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN75LVDS390PW	ACTIVE	TSSOP	PW	16	90	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDS390PWR	ACTIVE	TSSOP	PW	16	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDS390PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDT386DGG	ACTIVE	TSSOP	DGG	64	25	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDT386DGGR	ACTIVE	TSSOP	DGG	64	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDT388ADBT	ACTIVE	SM8	DBT	38	50	TBD	CU NIPDAU	Level-2-220C-1 YEAR
SN75LVDT388ADBTG4	ACTIVE	SM8	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDT388ADBTR	ACTIVE	SM8	DBT	38	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
SN75LVDT388ADBTRG4	PREVIEW	SM8	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDT390D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN75LVDT390DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
SN75LVDT390PW	ACTIVE	TSSOP	PW	16	90	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDT390PWR	ACTIVE	TSSOP	PW	16	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[(3)] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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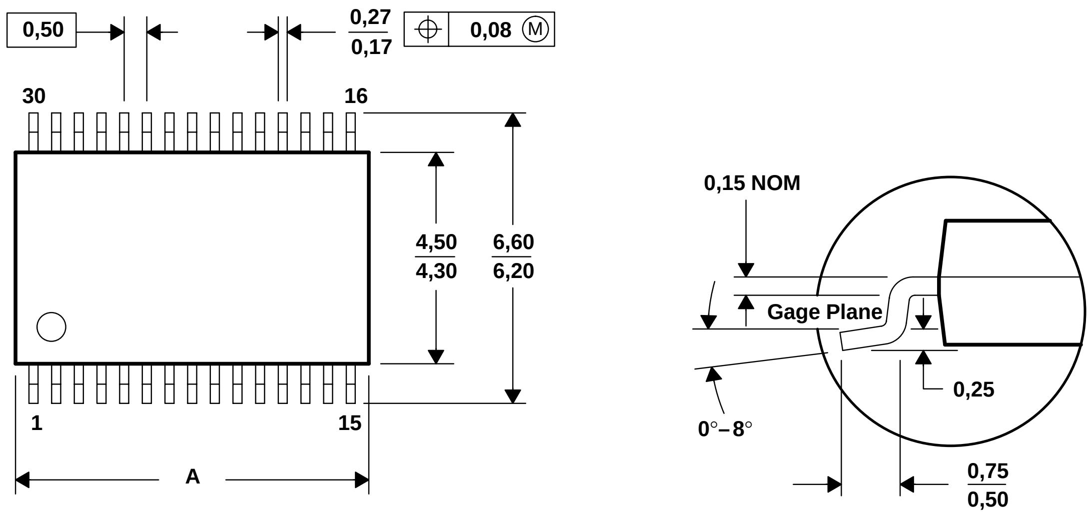
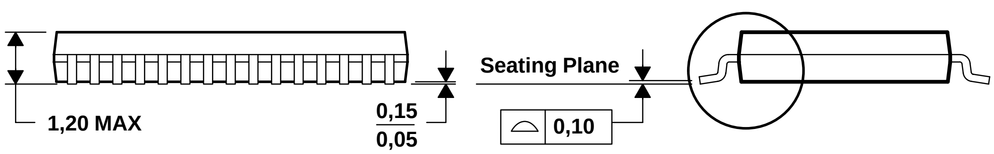
DBT (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

30 PINS SHOWN



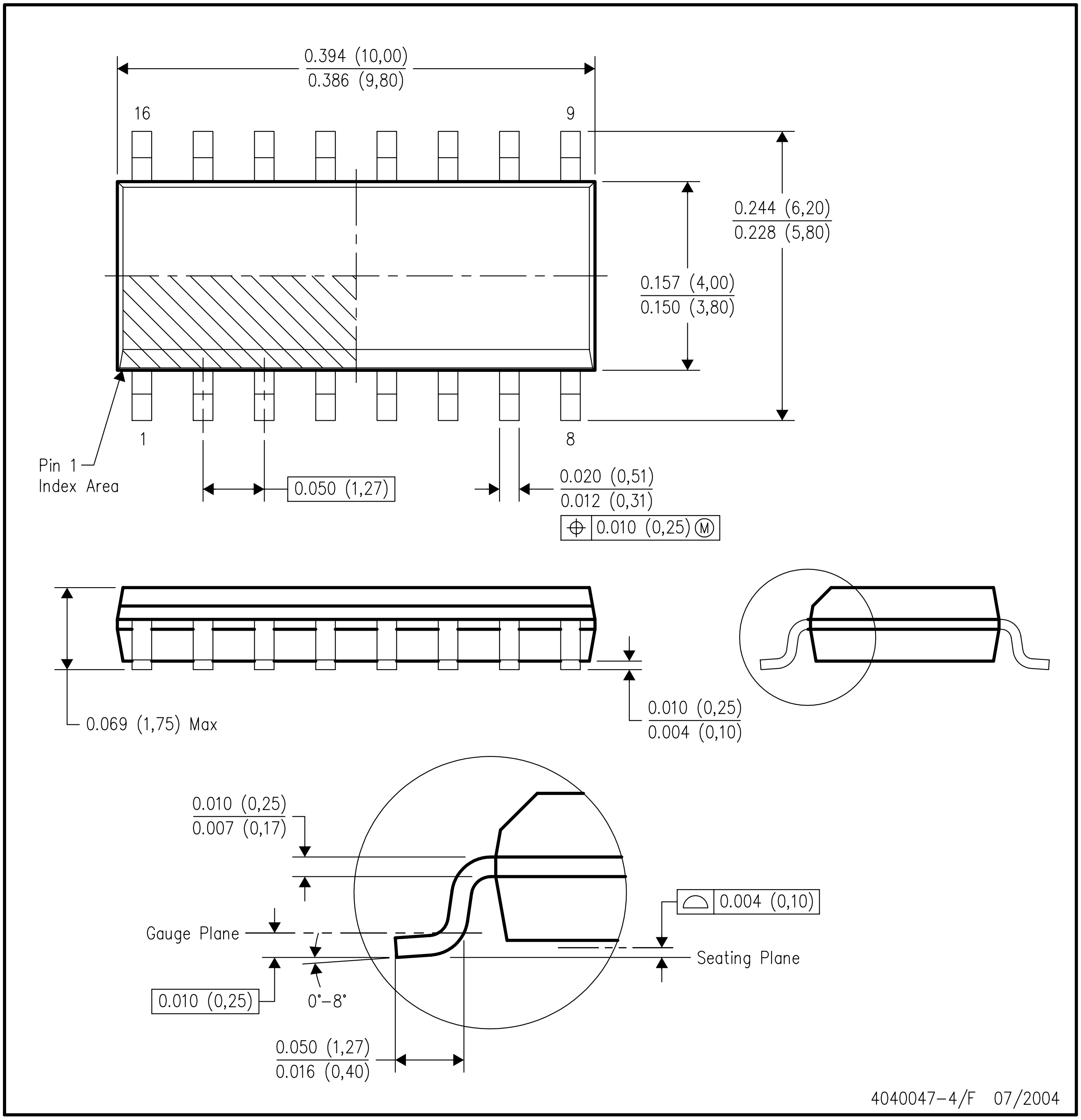


PINS ** / DIM	20	24	28	30	38	44	50
A MAX	5,10	6,60	7,90	7,90	9,80	11,10	12,60
A MIN	4.90	6,40	7,70	7,70	9,60	10,90	12,40

4073252/E 02/02

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153

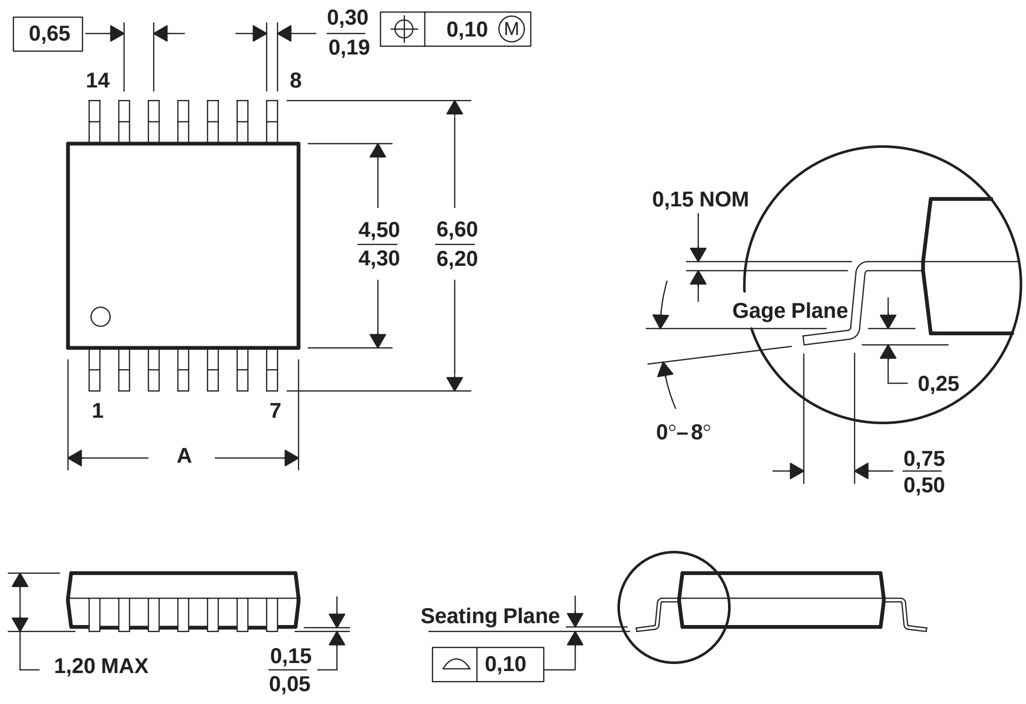
D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AC.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



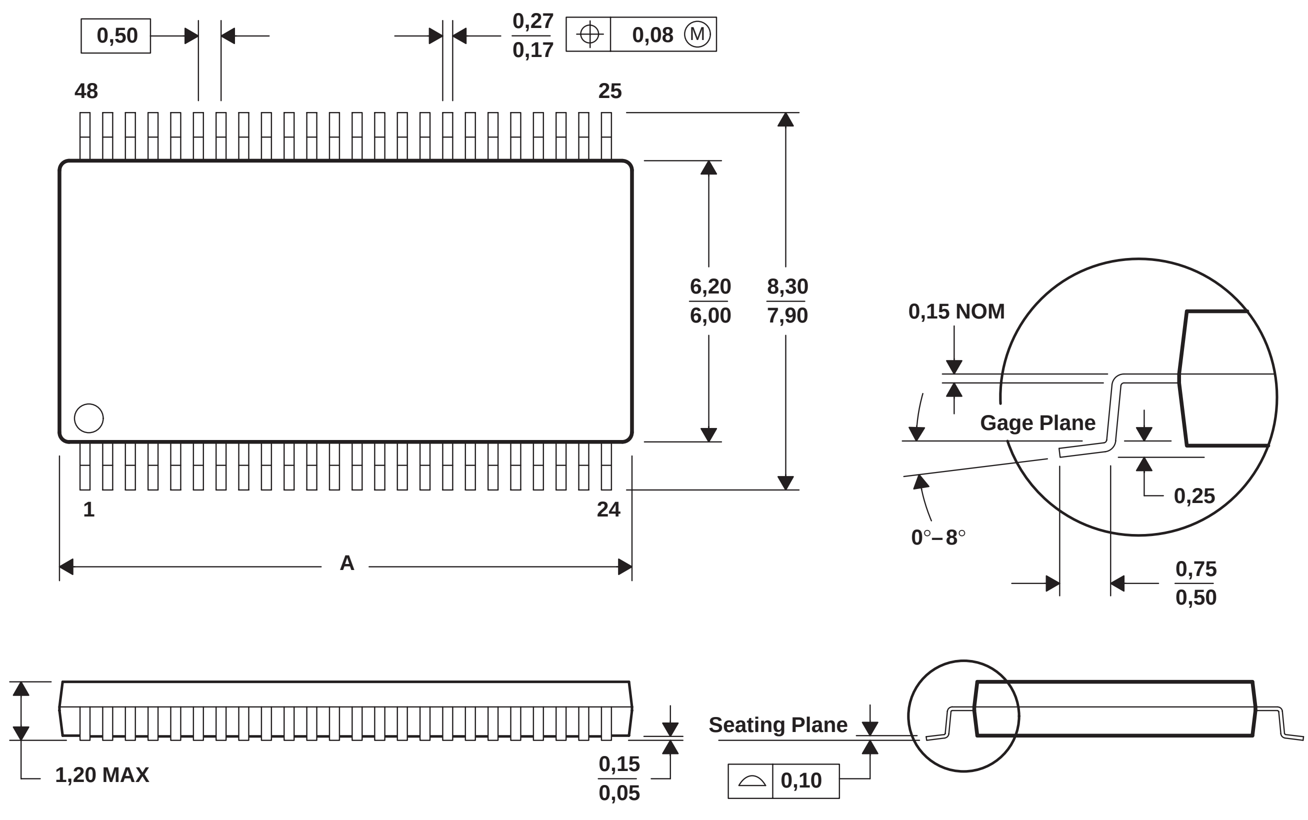
PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



PINS ** / DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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