RFMD
rfmd.com

Proposed

ML5830

LOW POWER INTEGRATED 5.8GHZ ASK/FSK TRANSMITTER

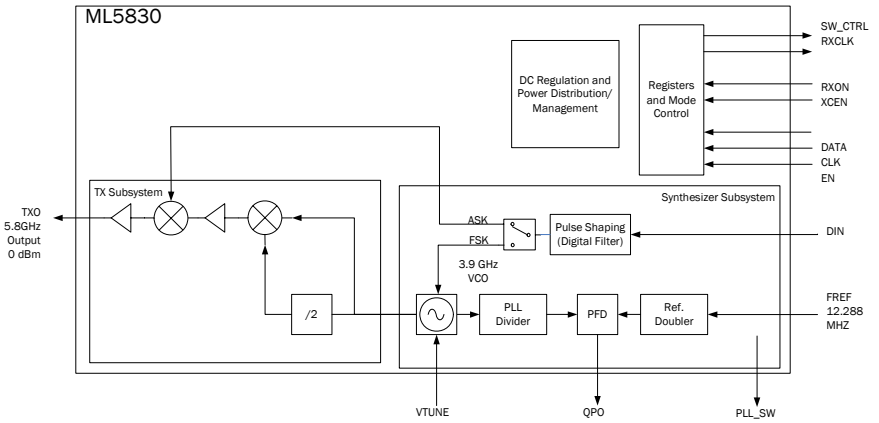
Package: QFN, 40-Pin, 6mmx6mm

Features

- Highly Integrated 5.8GHz, 512ksps to 2048ksps ASK and 2048ksps FSK Transmitter
- Fractional-N Synthesizer with 30Hz Resolution
- Fully Integrated Digital FIR TX Data Filter to Limit Occupied BW
- Self-calibrating VCO and Filters Eliminate Tuning
- ASK and FSK Modulation Modes
- +4dBm Output Power
- Includes FastWave™ Embedded Wireless Microcontroller Technology
- Simple 3-Wire Control Interface
- 40-Pin QFN Package (6mmx6mm)

Applications

- Electronic Toll Collection
- Wireless Data Links



Functional Block Diagram

Product Description

The ML5830 is a single chip fully integrated Amplitude Shift Keyed (ASK) and Frequency Shift Keyed (FSK) transmitter developed for a variety of applications operating in the 5.790GHz to 5.840GHz band.

The ML5830 ASK modulator is designed for symbol rates of 512ksps, 1024ksps, and 2048ksps. These ASK modulation symbol rates are required to support Biphase (FM0) encoded bit rates of 256kbps, 512kbps, and 1024kbps respectively. The FSK modulation symbol rate of 2048ksps supports a bit rate of 1024kbps with Manchester encoding.

The ML5830 RF path includes an upconversion mixer, a buffer/predriver, and an ASK modulator to produce a typical output power of +1dBm. A fully integrated fractional synthesizer with an FSK modulation function is used. Power supply regulation is included in the ML5830 providing circuit isolation and consistent performance over supply voltages between 2.8V to 3.6V.

Optimum Technology Matching® Applied

☐ GaAs HBT	☑ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Absolute Maximum Ratings

Parameter	Rating	Unit
VCC, VDD, VCCSYN, VCCPLL, VCCA, VCCA1	VSS-0.3 to 3.6	V
Junction Temperature	150	°C
Storage Temperature	-65 to +150	°C
Lead Temperature (Soldering, 10s)	260	°C
DM: Case Temperature	-20 to +55	°C
VCC, VDD, VCCSYN, VCCPLL, VCCA, VCCA1	2.8 to 3.6	V
Thermal Resistance	36	°C/W

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

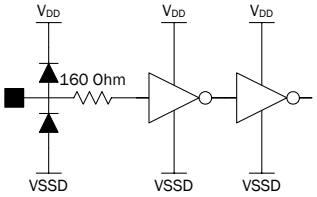
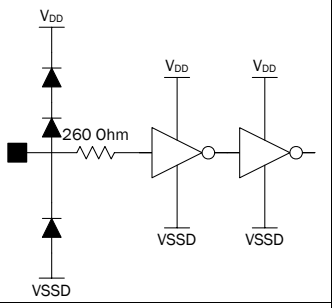
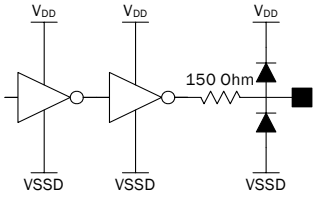
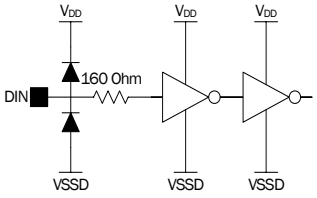
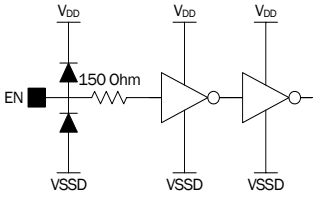
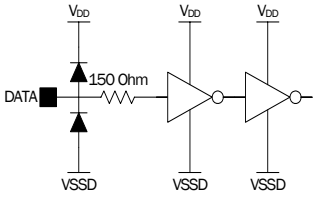
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Electrical Characteristics					Unless otherwise specified, T_C=25°C, and the supply voltage is V_{CC}=3.0V, F_{REF}=12.288MHz, PRBN BIT RATE=1024kbps, all measurements are normalized to the IC pins.
Power Supplies					
STANDBY Mode Current		0.3		µA	DC supply connected, all digital inputs low
IDLE Mode Current		29		mA	Calibration
Operating Current		51		mA	Normal mode
		36		mA	Low current mode
Synthesizer					
Charge Pump Sink/Source Current		±0.2		mA	
VCO Input Voltage	0.3		2.5	V	
Lock Time for Frequency Change		55		µsec	From EN asserted TXV
TXO Frequency Drift Rate		33	40	ppm/ms	Low current mode
Phase Noise (Normal Current Mode)		-85		dBc/Hz	@ 100kHz
		-116		dBc/Hz	@ 1MHz
		-121		dBc/Hz	@ 2MHz
		-133		dBc/Hz	@ 10MHz
Phase Noise (Low Current Mode)		-78		dBc/Hz	@ 100kHz
		-110		dBc/Hz	@ 1MHz
		-118		dBc/Hz	@ 2MHz
		-125		dBc/Hz	@ 10MHz
Reference Signal Frequency		12.288		MHz	
Reference Signal Input Level	0.5			V_{P-P}	Clipped sine, AC coupled
Transmitter					
Transmit Frequency Range	5.790		5.840	GHz	
TX Output Power		+4		dBm	Matched into 50Ω
FSK Modulation Deviation		±512		kHz	Symbol Rate=2048ksps
Output Impedance at 5.8GHz		43.7+j28.6		Ω	At TXO pin
Amplitude Modulation Index	0.5	0.8	0.9		All symbol rates

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

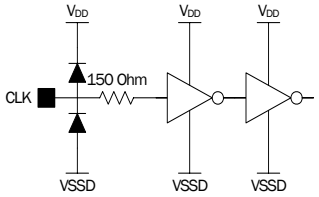
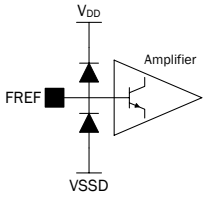
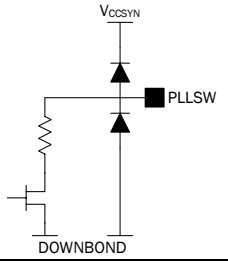
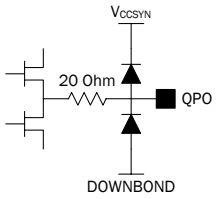
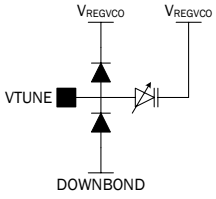
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Transmitter, cont.					
ASK Transmit Filter Bandwidth/Symbol Rate Ratio		0.9			Symbol Rate=1024ksps
		0.7			Symbol Rate=2048ksps
FSK Transmit Filter Bandwidth/Symbol Rate Ratio		0.7			Symbol Rate=2048ksps
Occupied BW, ASK Mode, 99% Power, 1MHz RBW		2.4	3.0	MHz	Symbol Rate=1024ksps
		2.8	3.5	MHz	Symbol Rate=2048ksps
Adjacent Channel Power, ASK Mode, 1MHz RBW, 5MHz Offset		-50	-30	dBc	Symbol Rate=1024ksps
		-45	-30	dBc	Symbol Rate=2048ksps
PLL Reference Spurious		-50		dBc	$V_{FREF}<2V_{P-P}$ clip-sine
TX LO Feed Through, LO Harmonics and Sub-Harmonics*		-40	-33	dBm	P_{TXO}=0dBm, F_{SPUR}=1/3, 2/3, 4/3, and 5/3 F_{TXO}
TX Harmonics, P_{TXO}=4dBm CW		-19	-15	dBm	2nd Harmonic
		-46	-33	dBm	3rd Harmonic
Interface Logic Levels					
CMOS Digital Input Pins (CE TXONB, DIN, DATASEL)					
Input High Voltage	V_{DD}*0.7		V_{DD}	V	
Input Low Voltage	0		V_{DD}*0.3	V	
Input Bias Current	-5		+5	µA	All states
Input Capacitance		4		pF	1MHz test frequency
CMOS Digital Output Pins (TXV, TXVB)					
Output High Voltage	V_{DD}*0.4			V	Sourcing 5.0mA
Output Low Voltage			0.4	V	Sinking 5.0mA
Source/Sink Current	±5.0	±8.0		mA	
3 Wire Serial Bus Timing					
CLK Input Rise Time (Note 1)			15	ns	
CLK Input Fall Time (Note 1)			15	ns	
CLK Period	50			ns	
EN Pulse Width	2000			ns	
Delay from last Clock Rising Edge to Rise of EN	15			ns	
EN Setup Time to Ignore next Rising	15			ns	
CLK					
Data-to-CLK Setup Time	15			ns	
Data-to-CLK Hold Time	15			ns	

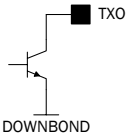
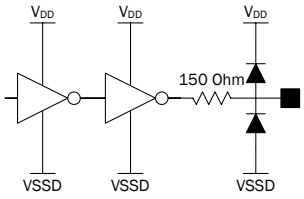
*TX frequency=F_{TXO}, TX power=P_{TXO}

Note 1: Serial I/O clock maximum rise and fall times are based on the minimum clock period. Longer rise and fall times can be accommodated for slower clocks provided the rise and fall times remain less than 20% of the clock period and all set up and hold time minimums are met with respect to the CMOS switching points (V_{IL} MAX and V_{IH} MIN). The serial I/O clock rise and fall times are limited to an absolute maximum of 100ns.

Pin	Function	Description	Interface Schematic
1	CE	Transmitter Enable input. Enables the bandgap reference and voltage regulators when high, enabling normal control functions. Consumes only leakage current in STANDBY mode when low. Operating mode=V_{IH} Standby mode=V_{IL}	
2	TXONB	TX Control Input. Switches the transmitter on. Idle mode=V_{IH} Transmit mode=V_{IL}	
3	TXV	Logic high (V_{OH}) while transmitting. Logic low (V_{OL}) while idle.	
4	DIN	Transmit Data Input.	
5	VSSD	Digital ground for all digital I/O circuits and control logic.	
6	EN	Control Bus Enable. Enable pin for the three-wire serial control bus. The control registers are loaded on the rising edge of this signal. Serial control bus data is ignored when this signal is high (V_{IH}).	
7	DATA	Serial Control Bus Data.	

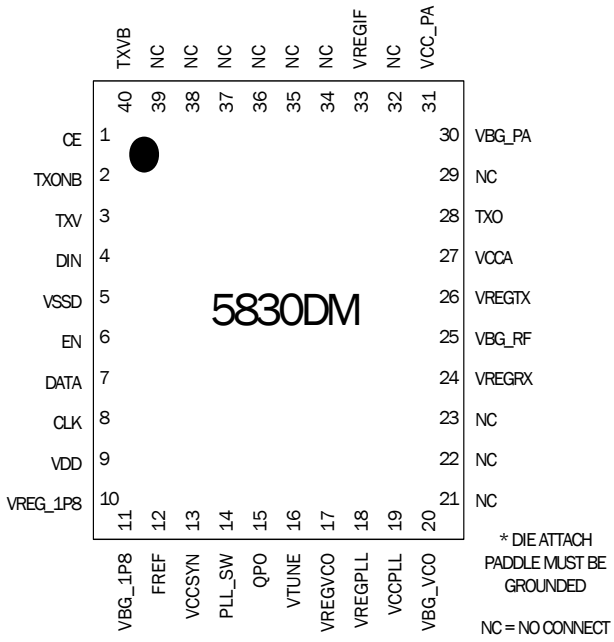
7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Pin	Function	Description	Interface Schematic
8	CLK	Serial control bus data is clocked in on the rising edge and only when EN is low.	
9	VDD	3.3V_{DC} power supply input.	
10	VREG 1P8	1.8V_{DC} regulator output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
11	VBG 1P8	1.13V_{DC} bandgap voltage output. Place capacitor between this pin and ground to decouple (bypass) noise.	
12	FREF	Input reference frequency.	
13	VCCSYN	2.7V_{DC} power supply input. Must be connected to VREGPLL pin externally.	
14	PLL SW	Loop filter control switch.	
15	QPO	Charge pump output of the phase detector. This is connected to the external PLL loop filter.	
16	VTUNE	VCO Tuning Voltage input from the PLL loop filter. This pin is very sensitive to noise coupling and leakage currents.	
17	VREGVCO	2.5V_{DC} regulator output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
18	VREGPLL	2.7V_{DC} power supply output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
19	VCCPLL	3.3V_{DC} power supply input. Place capacitor between this pin and ground to decouple (bypass) noise.	
20	VBG VCO	1.13V_{DC} bandgap voltage output. Place capacitor between this pin and ground to decouple (bypass) noise.	
21			

Pin	Function	Description	Interface Schematic
22			
23			
24			
25	VBG RF	Bandgap 1.24V decouple voltage. Decoupled to ground with a capacitor.	
26	VREGTX	2.7V_{DC} power supply input.	
27	VCCA	3.3V_{DC} power supply input.	
28	TXO	TX RF open-collector output. Connect this pin to VCC using an (RF blocking) inductor.	
29			
30			
31	VCCA1	3.3V_{DC} power supply input.	
32			
33			
34	TPI	Factory test pin - NC (do not connect).	
35	TPQ	Factory test pin - NC (do not connect).	
36	TPA	Factory test pin - NC (do not connect).	
37	TPB	Factory test pin - NC (do not connect).	
38			
39	DATASEL	Factory test pin - NC (do not connect).	
40	TXVB	Logic high (V_{OH}) while idle. Logic low (V_{OL}) while transmitting.	
Pkg Base	GND	Ground connection. The backside of the package should be connected to the ground plane through a short path, i.e., vias under the device will be required.	

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Pin Out



7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Functional Description

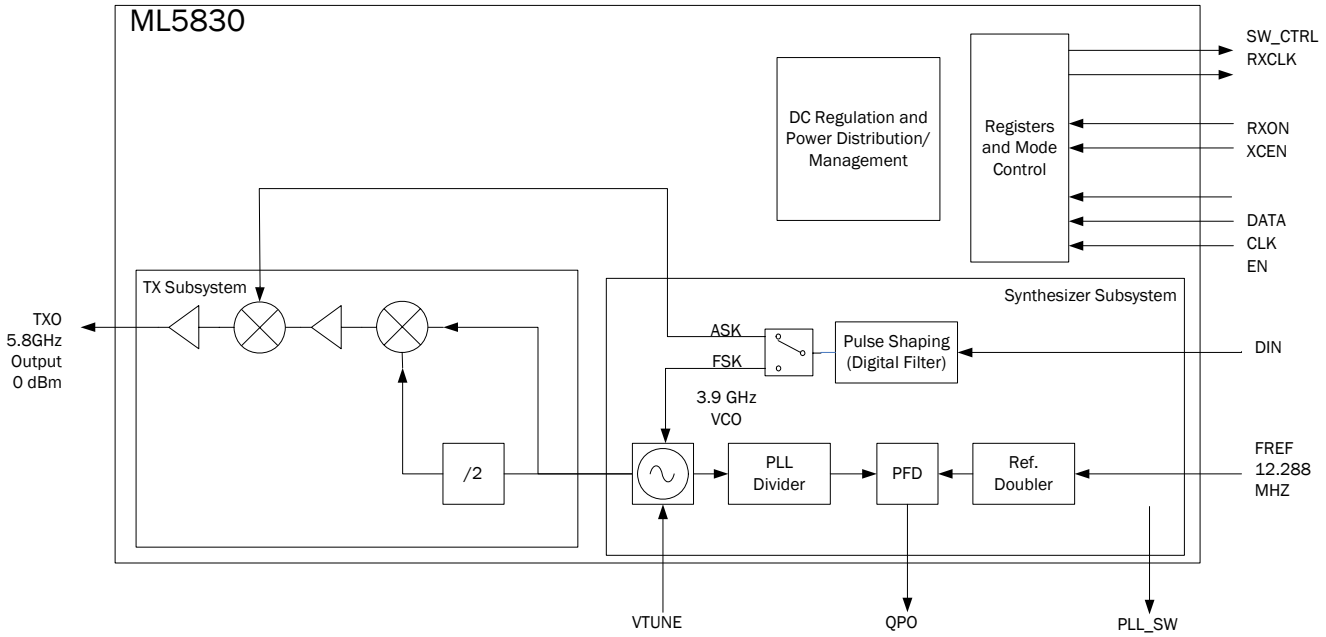


Figure 1: ML5830 Block Diagram

The ML5830 is a single chip digital wireless transmitter. The ML5830 integrates all the frequency synthesizer, modulation, and transmit functions to form a complete 5.790GHz to 5.840GHz ISM band radio. The ML5830 is designed to transmit CW, ASK, or FSK modulation from 512ksps to 2048ksps at any frequency over the 5.790GHz to 5.840GHz ISM band. The frequency synthesizer tuning resolution is 30Hz.

Automatic Alignment

The ML5830 is calibrated to remove process and temperature variation. Calibration occurs after: 1) the ML5830 is first powered on (V_{CC}>2.8V_{DC}), 2) the serial registers are written, and 3) CE is set high. Calibration can be suppressed in future CE cycles by initially setting the register 0 CALONCE bit to 1. Calibration is typically performed once per sleep/wake cycle or once minute of continuous operation (longer continuous periods are possible if temperature does not change).

Transmitter

The ML5830 transmitter consists of an up-conversion mixer followed by a programmable gain amplifier to allow factory calibration and ASK modulation of the output power. The input data is filtered before sent to an adjustment free VCO or ASK modulator. An FIR Gaussian pulse shaping filter is used followed by DAC and interpolation filter for clock rejection. The output of the ASK modulator is up-converted by a mixer and amplified to deliver +1dBm nominal output power.

PLL/Synthesizer

A single, on-chip 3.9GHz fractional-N synthesizer is used to generate the transmit carrier. The VCO has an on-chip resonator, active devices and tuning circuitry for a completely integrated VCO function. All required DC voltage regulation is within the IC. The PLL center frequency is programmed with a 23-bit word written via the SPI port during either standby or active operation. A lock detect circuit monitors the state of the PLL loop allowing the TX to be disabled prior to the PLL achieving lock.

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

The ML5830 has several modes of operation:

- STANDBY: All circuits off except digital control (static CMOS)
- IDLE: Voltage regulators and PLL are on, TX circuits off
- FSK: FSK transmit circuits are on
- ASK NORMAL: ASK transmit circuits are on with constant power
- ASK LOW CURRENT: ASK transmit circuits are on with active power management.

Mode Control

The operational modes are controlled by digital control inputs CE and TXONB and Register 0 bits ASK and CURRENTSAVE. CE is the chip enable/disable control pin, which sets the device to either operation or STANDBY modes. TXONB enables the transmitter circuits when held low. The behavior of the transmitter circuits is controlled by the serial control register settings. The relationship between the parallel control lines, the Register 0 bits and the mode of operation of the IC is summarized in Table 1.

Table 1: Modes of Operation

CE	TXONB	ASK	CURRENT SAVE	MODE NAME	FUNCTION
0	X	X	X	STANDBY	Control interfaces active, all other circuits powered down
1	1	X	X	IDLE	Regulator and PLL tuning are on but TX circuits are off
1	0	0	X	FSK	FSK transmit circuits are on
1	0	1	0	ASK NORMAL	ASK transmit circuits are on with constant power
1	0	1	1	ASK LOW CURRENT	ASK transmit circuits are on with active power management

STANDBY Mode

In STANDBY mode, all voltage regulators are off. The only active circuits are the digital control interfaces, which are static CMOS, powered directly to minimize power consumption. The serial control interface and control registers remain powered and will accept and retain programming data as long as the VCC, VCCA and VCCA1 are present.

IDLE Mode

In IDLE mode, voltage regulators are on and calibration will occur immediately after CE=1 and PLL tuning also takes place. If the CALONCE register bit is set to 1, only one calibration cycle will occur within each VCC cycle or if the RESET bit is set.

TRANSMIT Modes

In ASK NORMAL TRANSMIT mode, filtered ASK data may be transmitted for any time duration. Constant regulator current applied to all circuits.

In ASK LOW CURRENT TRANSMIT mode, filtered ASK data can be transmitted for at least 2 milliseconds (ms). Some voltage regulators are disabled during transmit to reduce battery drain. By selecting the voltage regulator by-pass capacitors shown in figure 5, frequency drift during transmit can be limited to +80ppm maximum at 27°C. For this mode of operation, CE must be set high 2ms before transmit (TXONB=0) during the calibration phase or first CE=1 event (see Table 2). For example, TX frequency should be offset by -80ppm to compensate for this drift.

In FSK TRANSMIT mode, a closed loop FSK modulator drives both the VCO and the fractional-N PLL. The VCO is directly modulated with digitally filtered FSK transmit data. The PLL is driven by a sigma-delta modulator, which ensures that the PLL follows the mean frequency of the modulated VCO. Constant regulator current applied to all circuits.

Control Interface
There are two types of input/output (I/O) signals to control and monitor the ML5830; discrete I/O and serial input.

- Discrete I/O: CE, TXONB, TXV, TXVB
- Serial Control Bus: EN, DATA, CLK

The ML5830 transmitter is used in time division duplex (TDD) mode, where the transmitters at each end of a radio link alternately transmit and receive.

RF Control: CE, TXONB
The CE pin enables/disables the ML5830 and places the device in either STANDBY or ACTIVE modes.

The TXONB pin determines which active mode the ML5830 is in: IDLE or TRANSMIT.

TXV and TXVB are complimentary CMOS outputs that signal the validity of the TX output. They can directly drive PIN diodes. TXV outputs logic high when TXONB is asserted low. The time delays between TXV and TXVB are programmable are shown in Figure 3 and Table 3. These outputs are inhibited when the PLL is not locked.

ML5830 Initialization after Power On (VCC=Low to High)
After power on, the microcontroller must first initialize the ML5830 configuration registers and PLL frequency word while CE=0. At a minimum, register # 0 and the PLL frequency register must be written. Other registers may be changed at this time, also. After registers are written, CE is asserted (high) for a period of 257 usec minimum to perform a one-time internal calibration. After this time, the CE signal may be de-asserted (CE=0) to save current.

ML5830 Operation after Initizalization
When CE is asserted after the initialization process discussed previously, the ML5830 can then transmit data in as little as 117 us. This process may be repeated any number of times while VCC is held high. The initialization process and subsequent packet transmission cycles are illustrated in Figure 2 Complete ML5830 Transmission Cycle.

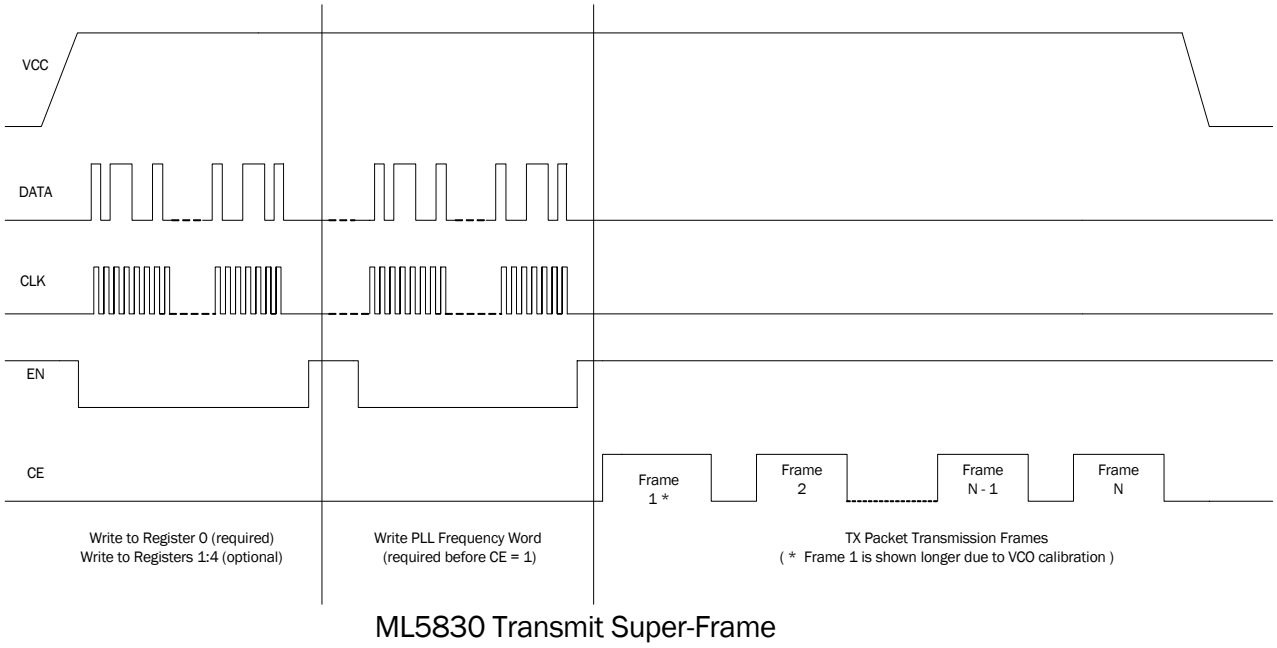


Figure 2: Complete ML5830 Transmission Cycle

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Packet Framing Methods for the ML5830

The ML5830 may be operated in one of three ways, differing in how the TX data packets are "framed" by the BBIC using either;

a. Transmit-On-Bar (TXONB) input and Transmit Valid or Transmit Valid Bar (TXV or TXVB) output signals,
b. CE framing along with the TXV or TXVB output signals, or
c. Unframed operation using data only.

Figure 3a Transmit Data Packet Timing illustrates these methods of packet framing.

Transmit Packet Framing using TXONB and TXV or TXVB (Figure 3a, Table 2)

Either 250 us or 110 us after CE=1 (depending on the state of the CALONCE bit), the TXONB signal can be used to enable and disable the transmitter and modulator. When TXONB=1 (not asserted), the transmitter and modulator are in standby, low current mode (the VCO and PLL are active, however). When TXONB=0 (asserted), the TX section powers on and issues the TXV and TXVB signals a short time later. TXV and TXVB are output to the BBIC as handshake feedback signals. Conversely, when TXONB is de-asserted (TXONB=1), the TX section turns off and TXV/TXVB revert also. Note, for low current mode operation, t_{WAKE1} changes from 250 us to 2000 us.

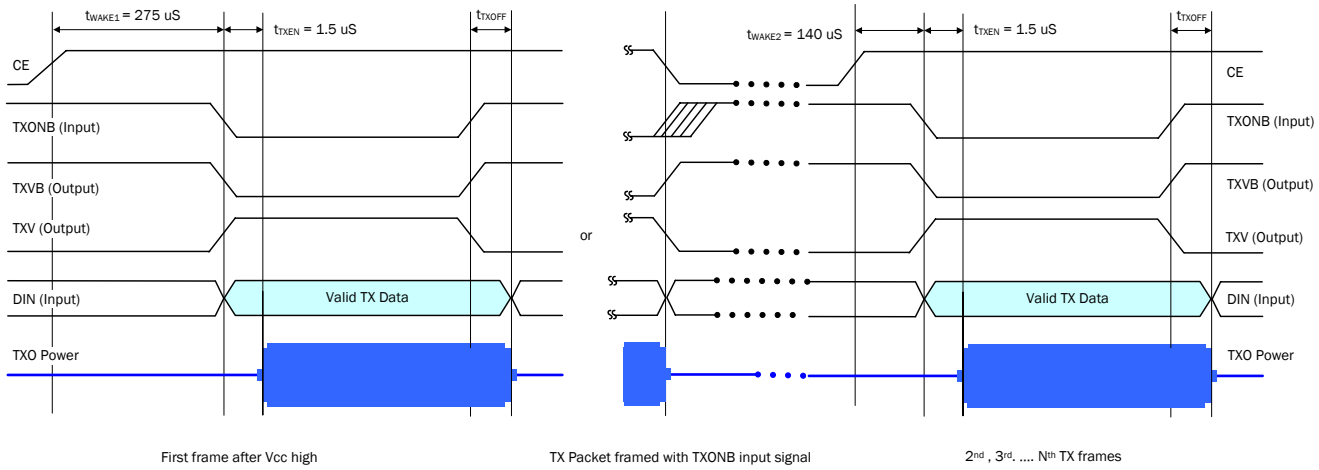


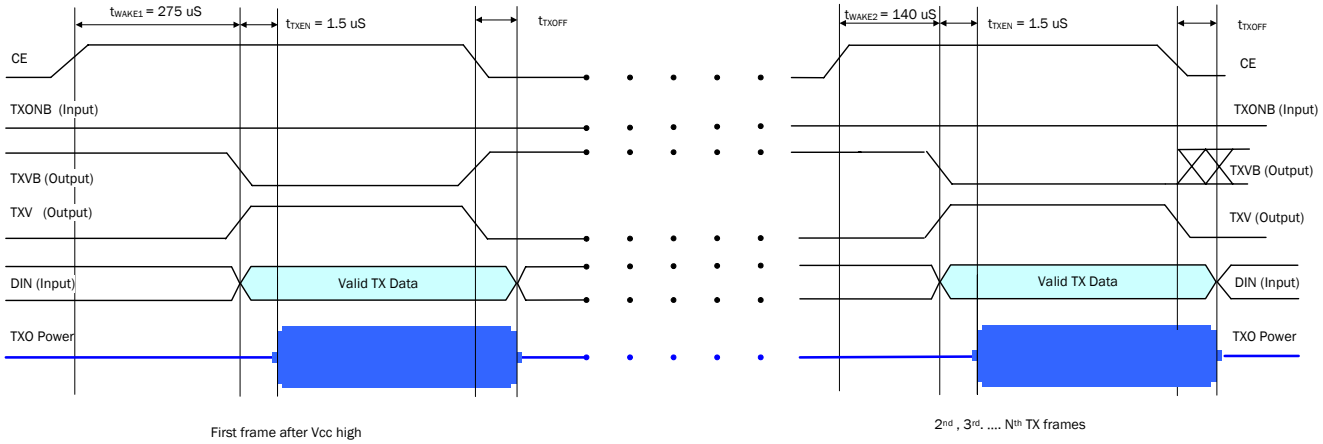
Figure 3a: Transmit Data Packet Timing

Table 2a: T_{WAKE1} Timing

SYMBOL	PARAMETER	TIME	UNITS
t_{WAKE1}	Delay from CE assertion to TXONB assertion, during first CE assertion after RESET in normal mode	250	µsec
t_{WAKE1}	Delay from CE assertion to TXONB assertion, during first CE assertion after RESET in low current mode	2000	µsec

Transmit Packet Framing using CE and TXV and TXVB (Figure 3b, Table 2)

Using this method, the TXONB signal is tied low. When CE is asserted, the transmitter PA and modulator will turn on in either 257 us or 117 us (depending on the state of the CALONCE bit) and the ML5830 then sends the TXV and TXVB output signals to the BBIC to indicate that the Tx is ready to send data. At the end of the transmission data packet, the BBIC pulls CE low, shutting down all analog functions (PA, modulator, VCO and PLL). This mode of framing produces the lowest current consumption. (This timing scheme can be used for normal mode operation. In low current mode, it cannot be use for the first packet but it can be used for subsequent packets.)

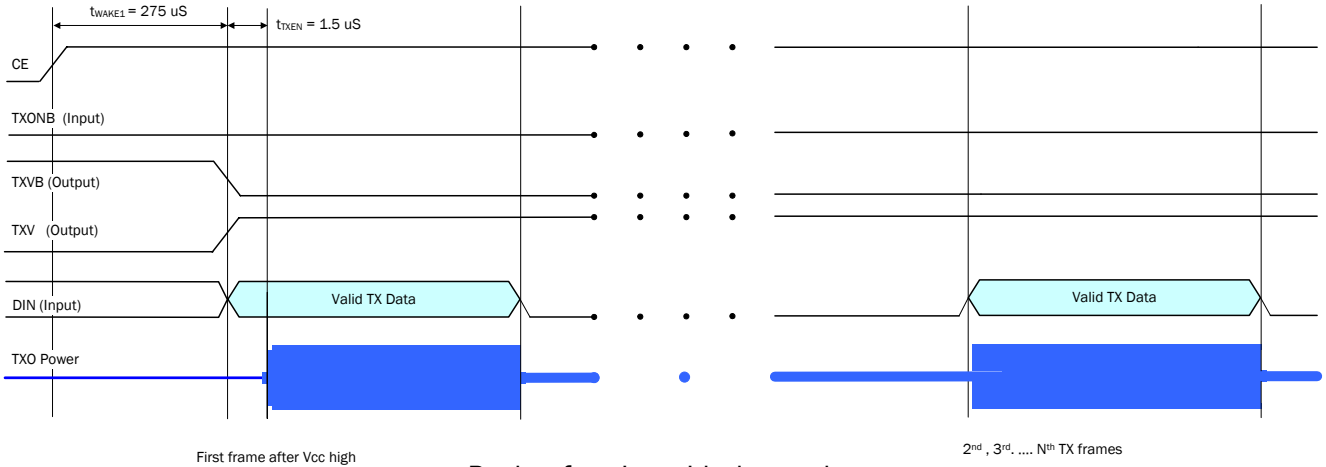


TX Packet framed with CE input and TXVB output
(using CE to start and stop the data packet frame)

Figure 3b Transmit Data Packet Timing

Unframed (packet framing using data only in normal mode, Figure 3c, Table 2)

In this mode, the BBIC sets CE=1 and TXONB=0 at all times (after initialization) to enable the transmitter PLL, VCO, PA and modulator. After the PLL is stable, the ML5830 and issues the TXV and TXVB output signals. The BBIC can either monitor TXV/TXVB or simply wait a fixed time and then begin transmitting data. Data may be transmitted at any time after this point with framing provided by the BBIC. All analog functions will then operate continuously on the ML5830.



Packet framing with data only
(CE input held high)

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Table 2b: Transceiver Control Interface Timing

SYMBOL	PARAMETER	TIME	UNITS
t_{TXEN}	Time from TXONB, TXV, and TXVB assertion to valid TX data out	7	µsec
t_{WAKE2}	Time from CE asserted to TXONB, TXV, and TXVB assertion during all other CE assertions if CALONCE=1	110	µsec
t_{TXOFF}	Time between falling edge of the TXV signal and falling edge of RF output power.	3.5 to 13.5	

Typical Transmit Current Profile

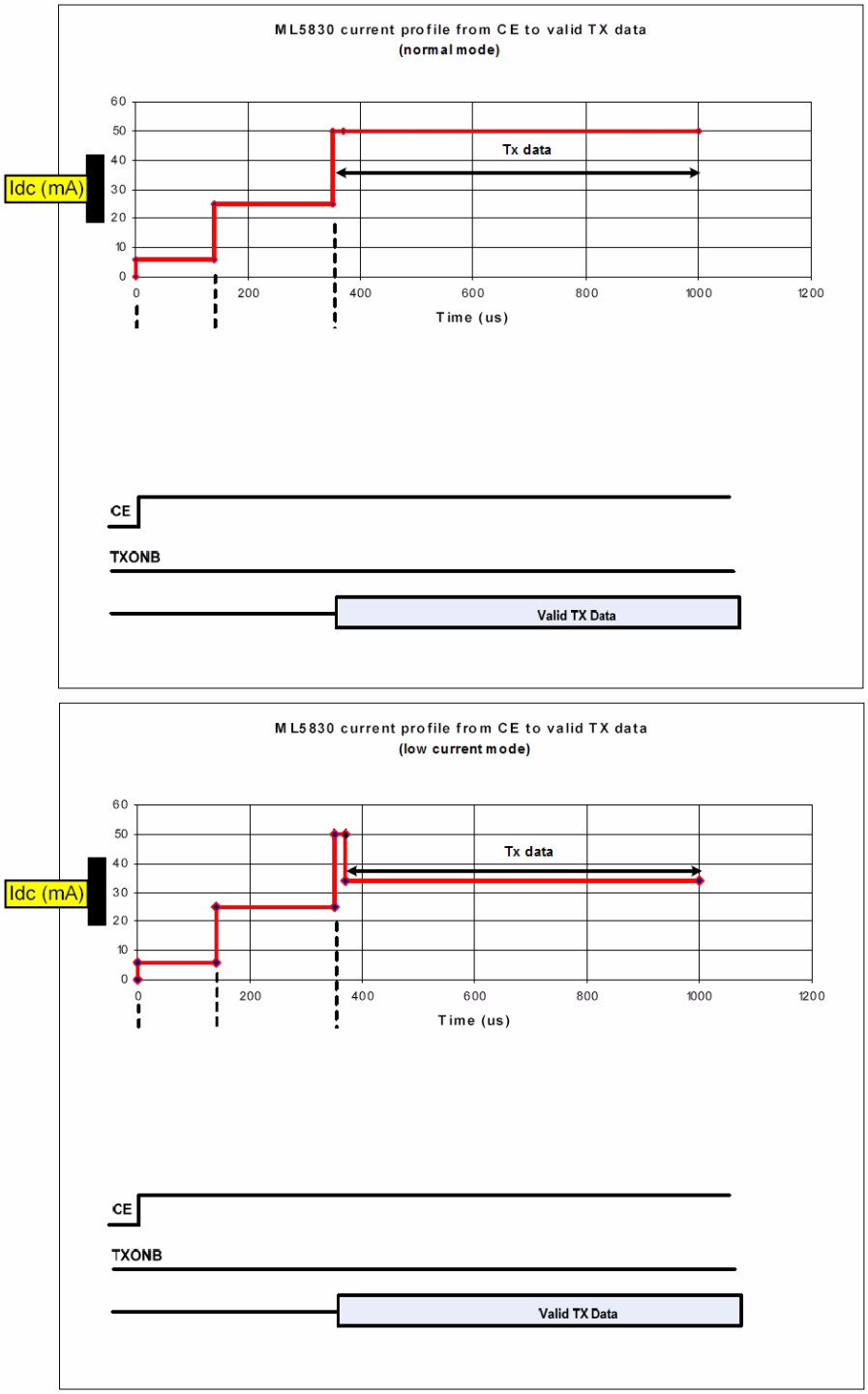


Figure 4: ML5830 TX Burst DC Current Profile. Initial power on case is shown. If CALONCE=1, the calibration cycle is omitted after first occurrence.

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Transmit Data Interfaces

There are two sets of transmit and receive data interfaces for the ML5830:

- Baseband Data: DIN, FREF
- RF Data: TXO

Please refer to application schematic in Figure 5 for recommended component values.

Baseband Data: DIN, FREF

The DIN pin is a CMOS logic level serial data input for ASK or 2-FSK modulation on the radio channel. This DIN pin drives data bits into the transmit modulator. There is no re-timing of the data bits, so the transmitted data bits take their timing from the DIN pin. However, the DIN signal is digitally sampled using the FREF clock (12.288MHz) and this clock must be used by the base band IC to generate data and avoid periodic setup and hold time violations that would cause data errors.

The 12.288MHz FREF pin is the master reference frequency (F_{REF}) input for the transmitter. It supplies the frequency reference for the RF channel frequency and the on-chip filter tuning. The FREF pin is a clipped sine input with on-chip biasing resistors. It can be driven by an AC coupled sine-wave or a CMOS logic source. FREF is used as a calibration frequency and as a timing reference in the control circuits. The reference source must be accurate to 20 PPM.

RF Data: TXO

The TXO transmit output is the only RF pin. The TXO pin requires a matching network for maximum power output into 50Ω (see Figure 5).

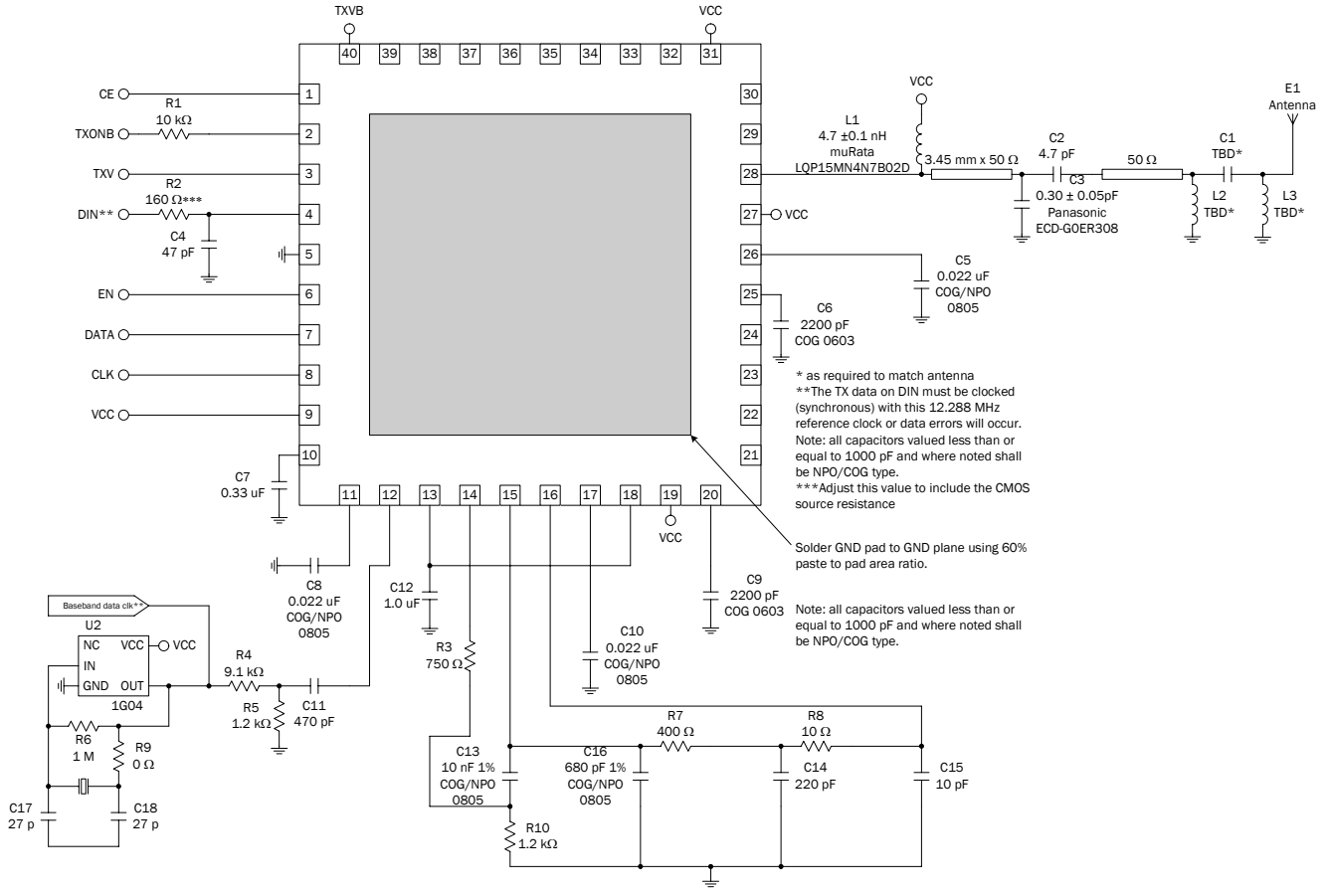


Figure 5: Application Schematic

Serial Bus Control: EN, DATA, CLK

A 3-wire serial interface is used for programming the ML5830 configuration registers, which control device mode of operation, pin functions, PLL and reference dividers, internal test modes and filter alignment. Data words are entered beginning with the MSB. The 24-bit configuration register word consists of 5-bit address and 16-bit data fields.. When the address field has been decoded the destination register is loaded on the rising edge of EN. Note: Providing less than 24-bits of data will result in unpredictable behavior when EN goes high.

Data and clock signals are ignored when EN is high. When EN is low, data on the DATA pin is clocked into a shift register by rising edges on the CLK pin. The information is loaded into the addressed latch when EN returns high. This serial interface bus is an industry standard bus commonly found on PLL devices. It can be efficiently programmed by either byte or 24-bit word oriented serial bus hardware. The data latches are implemented in CMOS and use minimal power when the bus is inactive (see Figure 6 and Table 3).

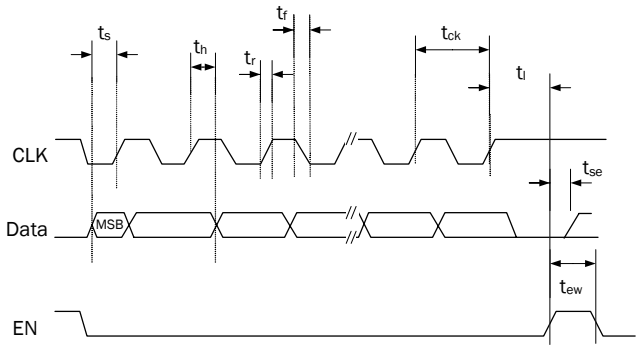


Table 3: Serial Bus Timing Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS
BUS CLOCK (CLK)				
t_r	Clock input rise time (Note 1)		15	ns
t_f	Clock input fall time (Note 1)		15	ns
t_{ck}	Clock period	50		ns
ENABLE (EN)				
t_{ew}	Minimum pulse width	2000		ns
t_l	Delay from last clock rising edge to rise of EN	15		ns
t_{se}	Enable set up time to ignore next rising clock	15		ns
BUS DATA (DATA)				
t_s	Data to clock set up time	15		ns
t_h	Data to clock hold time	15		ns

Note 1: Serial I/O clock maximum rise and fall times are based on the minimum clock period. Longer rise and fall times can be accommodated for slower clocks provided the rise and fall times remain less than 20% of the clock period and all set up and hold time minimums are met with respect to the CMOS switching points (VIL MAX and VIH MIN). The serial I/O clock rise and fall times are limited to an absolute maximum of 100ns.

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Serial Frequency Word and Configuration Registers

Serial Word Transaction Types and Configuration Register Map

Table 4: Serial Word Format (Frequency or Configuration Type)

Bit				
23	22	21	20:16	15:0
0	PLL Frequency Word			
1	RESET	WEN	ADDRESS	CDATA (see table 5)

Table 5: Configuration Register Map Showing ROM Default Values

Register (default)	Bit															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0		RATE	ASK	CURRENT SAVE	LOPWR	CAL ONCE	PLLUL ACT									
(0x263e	0*	0	1	0	0	1	1	0*	0*	0*	1*	1*	1*	1*	1*	0*
R1	DIVBASEOFFS										TXFILT EDGE	TXFILT POL				
(0x8487	1	0	0	0	0*	1*	0*	0*	1*	0*	0	0	0*	1*	1*	1*
R2									TTXOFF		TTXONA					
(0x158a)	0*	0*	0*	1*	0*	1*	0*	1*	1	0	0	0	1	0	1	0
R3																
(0x5505	0*	1*	0*	1*	0*	1*	0*	1*	0*	0*	0*	0*	0*	1*	0*	1*
R4	TXFILTSCALE								TTXOFFS							
(0x0080	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R5																
(0x000	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

* items are reserved.

Table 6: Configuration Register Variable Definitions

Signal Name	Width	Description
RATE	1	Selects data rate. 0≥1024kbps, 1≥2048kbps
ASK	1	Modulation type. 1≥ASK modulation, 0≥FSK modulation
CURRENTSAVE	1	Current save mode select. 0≥normal mode, 1≥current saving mode
LOPWR	1	0≥PLL is always on and active, 1≥PLL is off while TXONB is high
CALONCE	1	1≥calibrate only when the reset bit is set, 0≥librate each time CE goes high and TXONB is low at the same time
PLLULACT	1	0≥TX always enabled by TXONB, 1≥don't enable transmitter if the PLL is not locked
DIVBASEOFFS	4	DIVBASE offset
TXFILTEDGE	1	TX filter edge. 0≥clock on positive edge, 1≥clock on falling edge
TXFILTPOL	1	TX filter polarity. 0≥normal, 1≥invert filter polarity
TTXOFF	2	Delay time from TXV and TXVB until TX off. The delay will be 3.5µS+TTXOFF*40/*f ref* µS
TTXONA	6	Delay time from TXONB going low to TX on. The delay will be -8*TTXONA/(2*Fclk (in MHz)) µsx2
TXFILTSCALE	8	FSK and ASK modulation coefficient. ASK modulation index is set with this value and TXOFFS. In FSK mode, this value controls frequency deviation.
TTXOFFS	8	Ask modulation coefficiet offset (see TXFILTSCALE)

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Serial Word Formats

There are two types of serial words used, specified by the state of Bit 23. Bit 23=0 sets the serial word type to 'frequency' and Bit 23=1 specifies the serial transaction type as a 'configuration word'.

Bit	Definition
23	Specifies whether this serial transaction is type PLL frequency or type configuration register.
22:0	Data

Value	Definition
0	PLL frequency specification word
1	Configuration register specification word

PLL Frequency Word

The PLL Frequency Word may be sent during standby (CE=0) or operation (CE=1).

Bit	Value	Definition
23	0	Specifies PLL frequency word
22:20	IPART	Integer part of the PLL programming variable
19:0	FPART	Fractional part of the PLL programming variable

The frequency of the channel is controlled by the configuration PLL Frequency Word defined above and the input reference frequency. The expression for the channel frequency is

$$f_{ch} = 3f_{ref}\left[H + I + \frac{N}{2^{20}}\right]MHz$$

where;

N=FPART (the fractional part of the DSM programming value),

I=IPART (the integer part of the DSM programming value),

H=DIVBASEOFFS+147 for f_{ref}=12.288MHz,

DIVBASEOFFS=a variable defined in Register 3 (default=8),

f_{ref}=12.288MHz

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Configuration Register Serial Word

The configuration registers are written only during standby mode (CE=0). These data registers are volatile and will erase when VCC is removed. The format is shown below.

Bit	Value	Definition
23	1	This is a configuration register transaction.
22	RESET	
21	1	Must be set to write to register.
20:16	ADDRESS	Register address (value=0, 1, 2, 3, or 4)
15:0	CDATA	Configuration Register data.

Value	Definition
0	Normal operation
1	Perform reset operation. Must be asserted on first serial transfer.

All registers (R0, R1, R2, R3, and R4) will be loaded with default values and need to be initialized by the system base band hardware for the data rate used. See Table 6 following this section.

REGISTER 0

Register 0 is a special register because some of the hardware is controlled directly from this register. Since those specific bits are connected physically to active hardware, they must always be written first after power on. If Register 0 is not initialized first by the base band hardware, the ML5830 will not operate correctly.

Recommended Configuration Register Values

Table 7: Recommended Register Values for Each Data Rate

Register	Symbol Rate (ksps) and Modulation Type			
	512 ASK	1024 ASK	2048 ASK	2048 FSK
R0	0x247e	0x247e	0x647e	0x447e
R1	0x8487	0x8487	0x8487	0x8487
R2	0x3f00	0x3f00	0x3f00	0x3f00
R3	0x558b	0x558b	0x558b	0x558b
R4	0x8746	0x8746	0x8746	0x5f7f
R5	0xf818	0xf818	0xf818	0x7818

Please consult with RFMD application engineering for updates to these values or if you have special configuration requirements.

ML5830 Application to Electronic Toll Collection (ETC)

Using the ML5830 in an ETC system On Board Unit (OBU)

A typical ETC OBU system includes; an ML5830 ASK transmitter, a microcontroller (uP) or Base Band IC (BBIC), and a separate RF receiver circuit (see Figure 6 Typical OBU RF System Block Diagram). The BBIC performs baseband communication functions and controls the ML5830 using a SPI port for serial configuration, and several other discrete signals. The receive circuitry serves two functions; 1) it detects RF energy from the Road Side Unit (RSU) toll collection station and then "wakes up" the OBU from sleep mode and 2) demodulate the ASK coded information in the RSU transmissions. The RSU wake-up RF bursts are generated either periodically or by detecting traffic passing a particular point in the road.

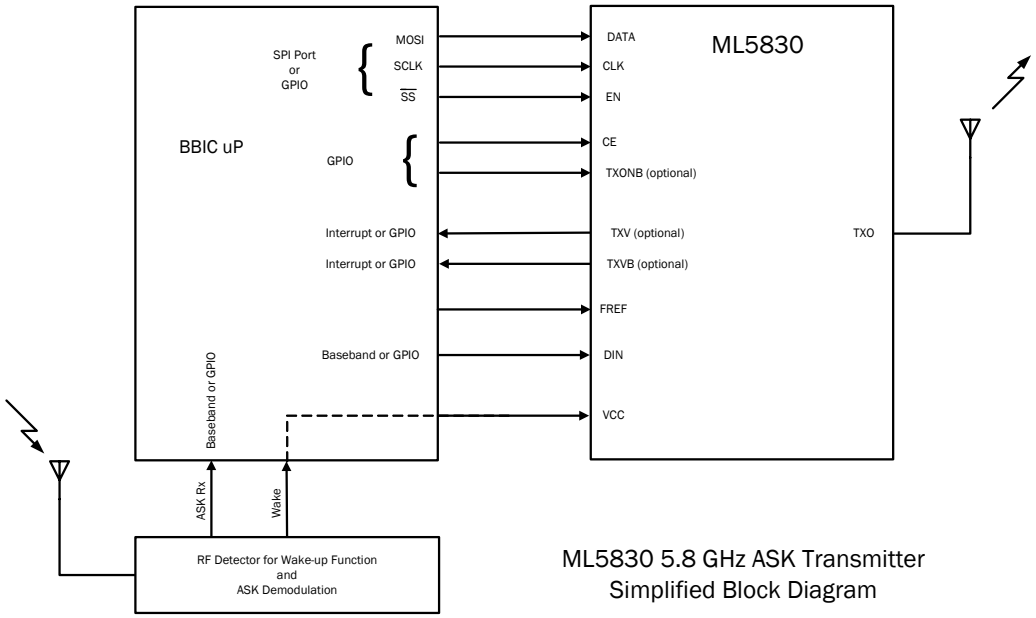


Figure 6: Typical OBU RF System Block Diagram

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

China ETC Mac Layer Timing Requirements

For reference, the China ETC MAC layer timing requirements, related to OBU transmitter operation, are shown below.

(Source: GB/T 20851.2-2007 Electronic toll collection - Dedicated short range communication-Part 2: data link layer)

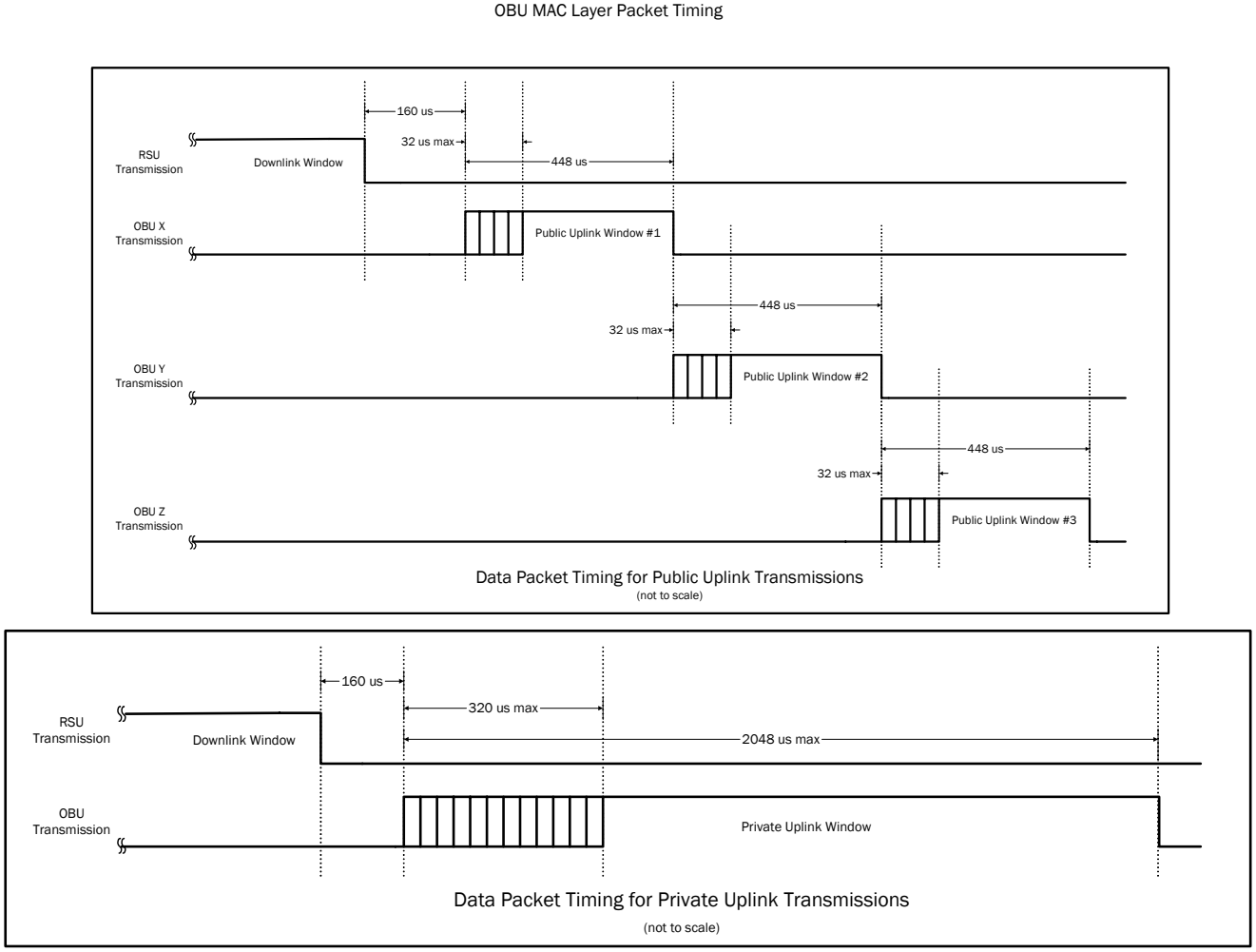
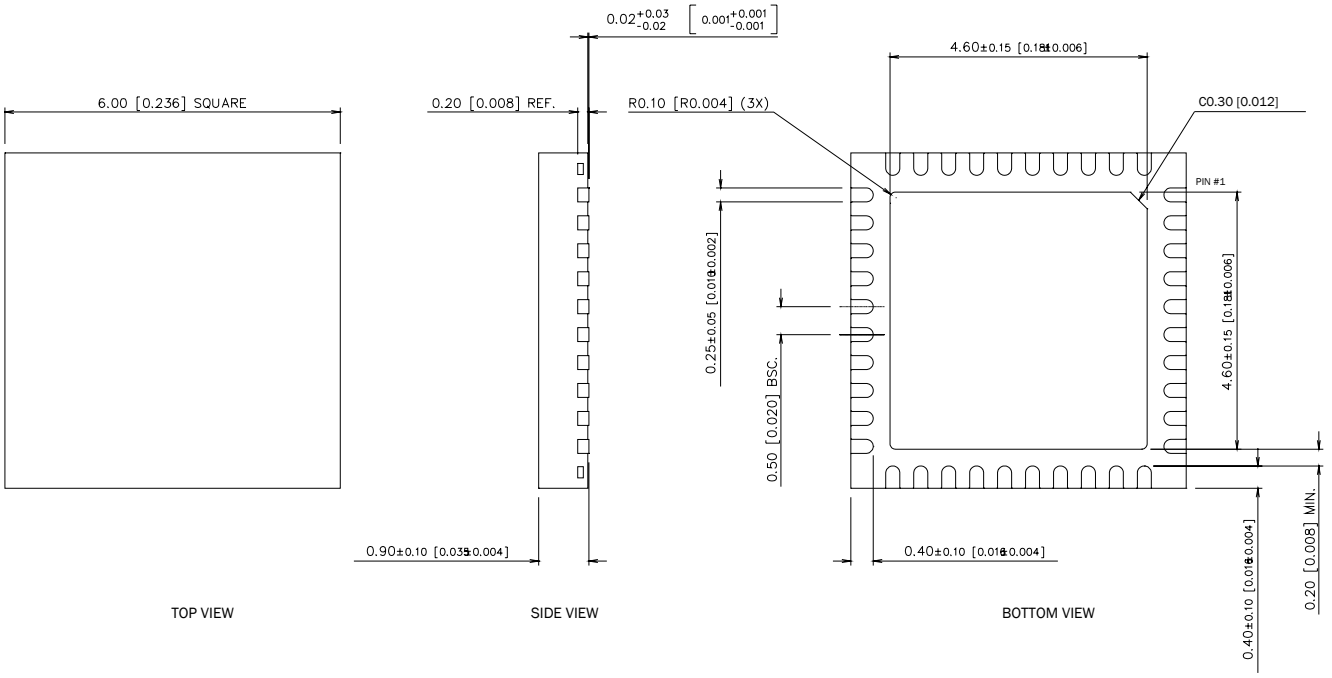


Figure 7: ETC MAC Layer Timing Requirements for OBU Transmit

Physical Dimensions



NOTES:
1. JEDEC REFERENCE: MO-220 (VJJD-4)
2. ALL DIMENSIONS ARE IN MM [INCHES].
3. GENERAL TOLERANCE: ±0.05 [±0.002]

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Ordering Information

Part Number	Temp Range	Package	Pack (Qty)
ML5830DM	-20°C to +55°C	40-Pin QFN 6mmx6mm	Antistatic Tray (490)
ML5830DM-T	-20°C to +55°C	40-Pin QFN 6mmx6mm	Tape and Reel (2500)

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.