NT6880

Keyboard Controller

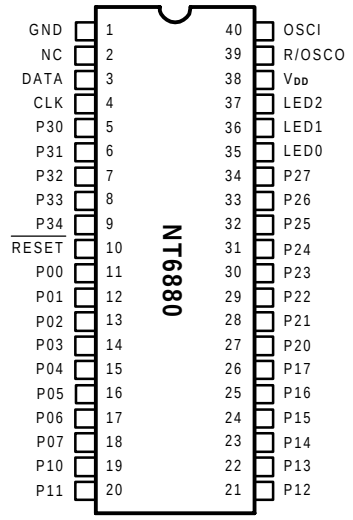
Features

- Built-in 6502 8-bit CPU
- 2 MHz CPU operation frequency
- 5K bytes of ROM
- 160 bytes of SRAM
- One 8-bit programmable base timer with 1 - 256 μsec interval
- 29 programmable bi-directional I/O pins
- 3 LED direct sink pins
- Mask optional for built-in RC oscillator with an external resistor or external ceramic resonator applied
- Mask optional for DATA/CLK driving capability
- Watch-dog timer reset
- Built-in power-on reset
- Built-in low voltage reset
- CMOS technology for low power consumption
- Available in 40 pin DIP package and 40 pad Chip Form

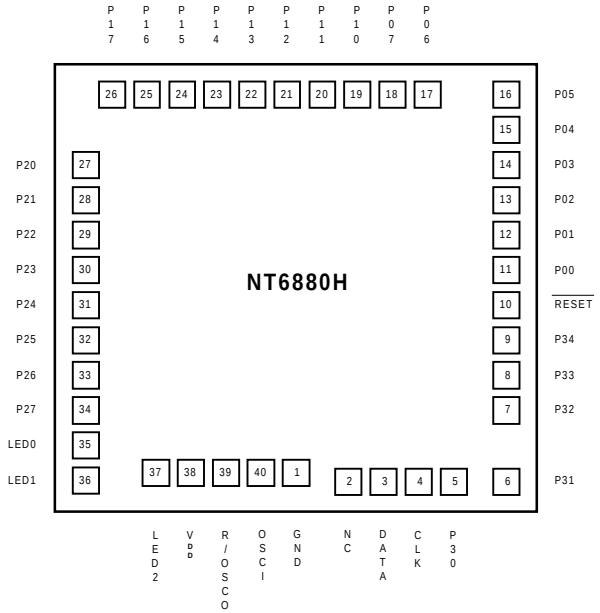
General Description

The NT6880 is a single chip micro-controller for keyboard applications. It incorporates a 6502 8-bit CPU core, 5K bytes of ROM and 160 bytes of RAM used as working RAM and stack area. It also includes 29 programmable bi-directional I/O pins and one 8-bit pre-loadable base timer. Additionally, it includes a built-in low voltage reset, a 4MHz RC oscillator requiring an externally applied resistor or a 4MHz ceramic resonator and a watch-dog timer that prevents system standstill.

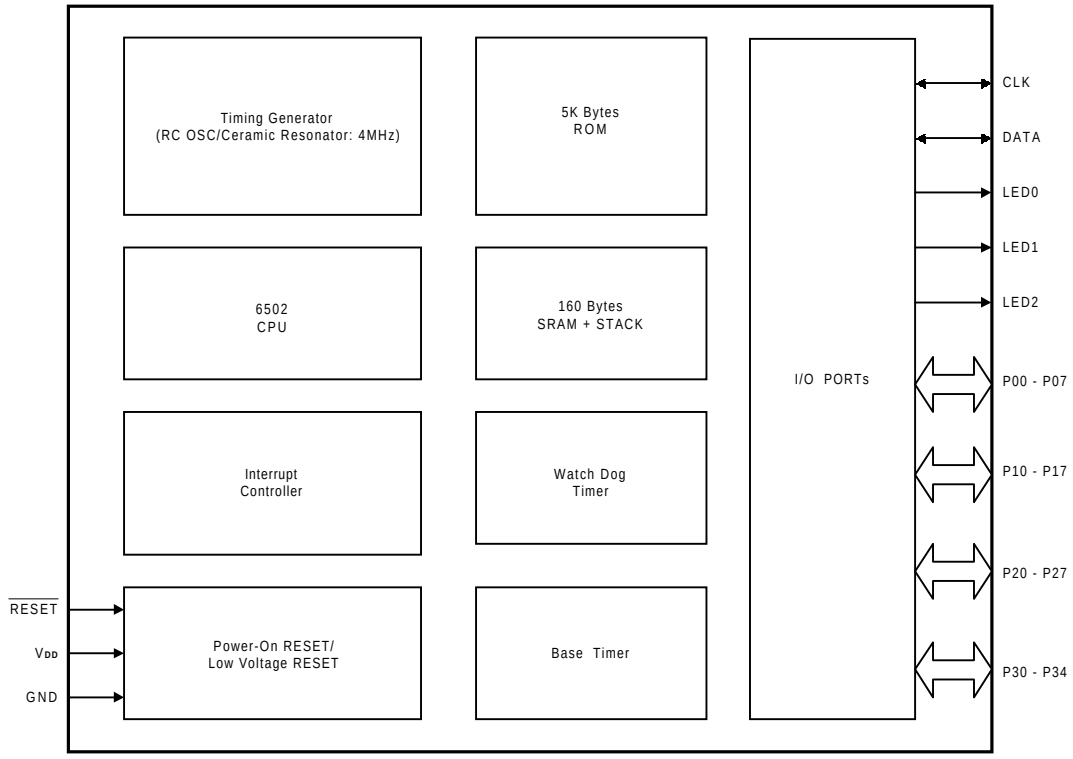
Pin Configuration



Pad Configuration



Block Diagram



Pin and Pad Descriptions

Pin No.	Pad No.	Designation	I/O	Description
1	1	GND	P	Ground pin
2	2	NC	-	No connection, recommended to connect V_{DD} or floating
3	3	DATA	I/O	I/O, 10KΩ pull-up resistor for communication
4	4	CLK	I/O	I/O, 10KΩ pull-up resistor for communication
5 - 9, 11 - 34	5 - 9, 11 - 34	P30 - P34, P00 - P27	I/O	Bi-directional I/O pins
10	10	$\overline{\text{RESET}}$	I	$\overline{\text{RESET}}$ signal input pin with internal pull up resistor; Active low
35 - 37	35 - 37	LED0 - LED2	O	LED direct sink pins
38	38	V_{DD}	P	Power supply
39	39	R/OSCO	I	47KΩ resistor connected for RC OSC or 4MHz ceramic resonator connected
40	40	OSCI	-	No connection for RC OSC connected for 4MHz ceramic resonator

* Under the constraint of the maximum frequency variation, $(\Delta F/F)_{max}$, ≤ ±1%, code 3, 7 (ceramic resonator option) must be selected and pin 39 and pin 40 must be connected to a ceramic resonator. If $(\Delta F/F)_{max}$, ≤ ±10%, code 1, 5 (RC OSC option) it is recommended that pin 39 be connected to a 47KΩ resistor with ≤ ±1% accuracy to V_{DD}. Pin 40 is floating.

Functional Description

1. 6502 CPU

The 6502 is an 8-bit CPU. Please refer to the 6502 data sheet for more details.

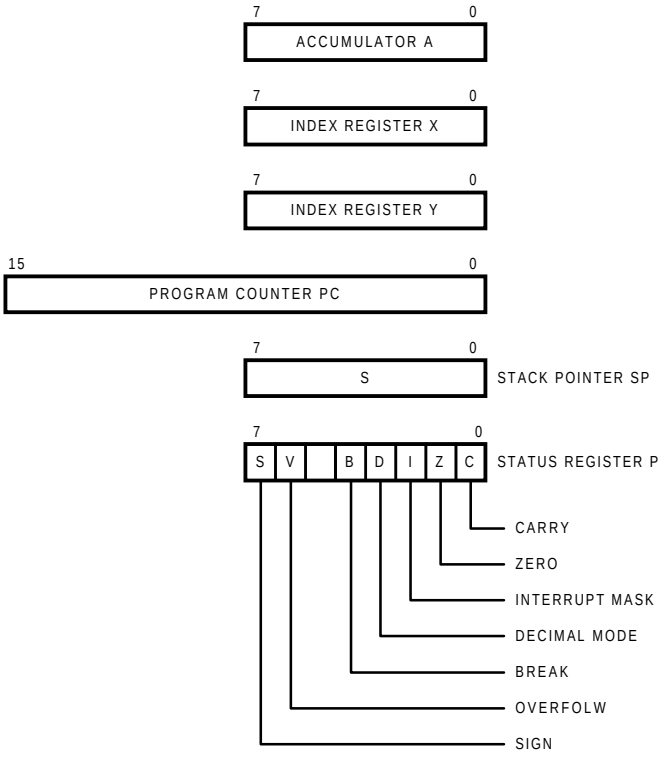


Figure 1.1 6502 CPU Registers and Status Flags

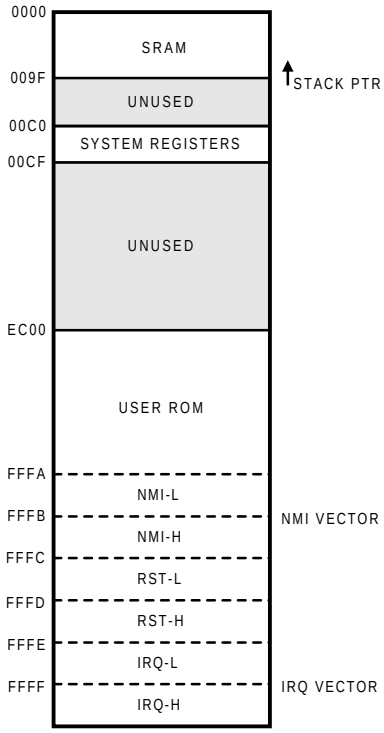


Figure 1.2. NT6880 Memory Map

2. System Reserved Registers

Addr.	Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
$00C0	BT	BT7	BT6	BT5	BT4	BT3	BT2	BT1	BT0	W
$00C1	TCON	-	-	-	-	-	-	-	$\overline{\text{ENBT}}$	W
$00C2	CLRIRQX	-	-	-	-	-	-	-	CLRIRQTMR	W
$00C3	PORT0	PD07	PD06	PD05	PD04	PD03	PD02	PD01	PD00	RW
$00C4	PORT1	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	RW
$00C5	PORT2	PD27	PD26	PD25	PD24	PD23	PD22	PD21	PD20	RW
$00C6	PORT3	-	-	-	PD34	PD33	PD32	PD31	PD30	RW
$00C7	CLK	-	-	-	-	-	-	-	CLK	RW
$00C8	DATA	-	-	-	-	-	-	-	DATA	RW
$00C9	LED	-	-	-	-	-	LED2	LED1	LED0	W
$00CA	CLRWDT	0	1	0	1	0	1	0	1	W
$00CB	X	X	X	X	X	X	X	X	X	X
$00CC	X	X	X	X	X	X	X	X	X	X
$00CD	X	X	X	X	X	X	X	X	X	X
$00CE	X	X	X	X	X	X	X	X	X	X
$00CF	X	X	X	X	X	X	X	X	X	X

- : no effect X : access not allowed

3. ROM: 5K X 8 bits

The built-in ROM program code, executed by the 6502 CPU, has a capacity of 5K X 8 bits and is addressed from **EC00H** to **FFFFH**.

4. SRAM: 160 X 8 bits

The built-in SRAM is used for general purpose data memory and for the stack area. SRAM is addressed from 0000H to **009FH**. User can allocate stack area in the SRAM by setting stack pointer register (S). Because the 6502 default stack pointer is 01FFH, it must be mapped to **009FH**. Mapping from 01XX to 00XX is done internally by setting the S register to **9FH** via software programming.
For example :

```
LDX   #$9F
TXS
```

For compatibility to UM6868A with 128-byte SRAM, the user's source code can not be changed.
For example :

```
LDX   #$7F
TXS
```

5. Power-On Reset

Built-in power-on reset circuit can generate a 150ms pulse to reset the entire chip. The beginning of the 150ms pulse occurs at 60% of V_{DD} when powered on.

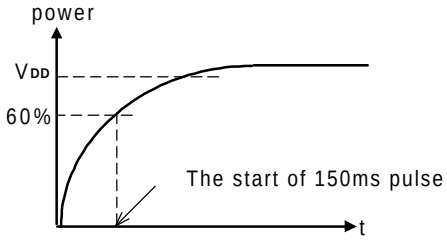


Figure 5.1. Power-On Reset Timing

6. Timing Generator

This block generates the system timing and control signal supplied to the CPU and on-chip peripherals. There are two types of system clock sources: built-in RC oscillator or external ceramic resonator. Both are mask optional and generate a 4MHz system clock. They also generate 2MHz for the CPU, and 1 MHz for base timer.

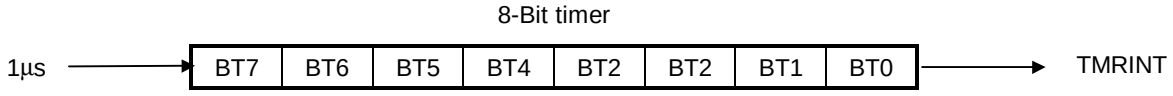
The following table provides the relationship between external resistor and RC OSC frequency. (for reference only)

External Resistor (KΩ)	RC OSC Frequency (MHz)
39	4.7
43	4.44
47	4
56	3.68

7. Base Timer (BT)

The base timer is an 8-bit counter with a 1MHz clock source. The base timer can be enabled/disabled by CPU. After reset, the base timer is disabled and cleared. The base timer can be preset by writing BT7 - BT0 to the BT register at any time. When enabled, the base timer starts counting from the preset value. When the value reaches FFH, it generates a timer interrupt if the timer interrupt is enabled. When it reaches the maximum value of FFH, the base timer will wrap around and begin counting at 00H. The timer interval can be programmed from 1 - 256 μsec. The base timer can be enabled by writing a '0' to '$\overline{\text{ENBT}}$' in the TCON (Timer Control) register. The $\overline{\text{ENBT}}$ is a level trigger.

Base timer structure:



BT pre-load data:

Addr.	Bit	7	6	5	4	3	2	1	0	R/W
$00C0	BT	BT7	BT6	BT5	BT4	BT3	BT2	BT1	BT0	(W)

Timer Control Register:

$00C1	TCON	-	-	-	-	-	-	-	$\overline{\text{ENBT}}$	(W)

8. Interrupt Controller

When a BASE TIMER overflow occurs, it will set the IRQTMR flag. The IRQTMR flag cannot be directly accessed by the software. Once set by an interrupt source, it remains High unless cleared by writing '1' to the corresponding bit in CLRIRQX ($00C2H). This register is cleared to '0' on initialization by a system reset.
When an interrupt occurs, the CPU will jump to $FFFEH & $FFFFH to execute an interrupt service routine. When the BASE TIMER interrupt occurs and enters an interrupt service routine, the IRQTMR flag must be cleared by the software.

Interrupt Control Register:

Addr.	Bit	7	6	5	4	3	2	1	0	R/W
$00C2	CLRIRQX	-	-	-	-	-	-	-	CLRIRQTMR	(W)

9. I/O PORTs

The NT6880 has 31 pins dedicated to input and output. These pins are grouped into 6 ports, as follows:

9.1. PORT0: (P00 - P07)

PORT0 is an 8-bit bi-directional CMOS I/O port that is internally pulled High by PMOS. Each pin of PORT0 can be bit programmed as an input or output pin under the software control. When programmed as output, data is latched to the port data register and output to the pin. PORT0 pins with "1" written to them are pulled high by the internal PMOS pull-ups, and are used as inputs in that state. These input signals can then be read. The port output is High after reset.

9.2. PORT1: (P10 - P17): Functions are the same as PORT0.

9.3. PORT2: (P20 - P27) : Functions are the same as PORT0.

9.4. PORT3: (P30 - P34) : Functions are the same as PORT0.

CLK & DATA : These two pins have the same structure as I/O ports.

PORT Registers:

Addr.	Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
$00C3	PORT0	PD07	PD06	PD05	PD04	PD03	PD02	PD01	PD00	(RW)
$00C4	PORT1	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	(RW)
$00C5	PORT2	PD27	PD26	PD25	PD24	PD23	PD22	PD21	PD20	(RW)
$00C6	PORT3	-	-	-	PD34	PD33	PD32	PD31	PD30	(RW)
$00C7	CLK	-	-	-	-	-	-	-	CLK	(RW)
$00C8	DATA	-	-	-	-	-	-	-	DATA	(RW)

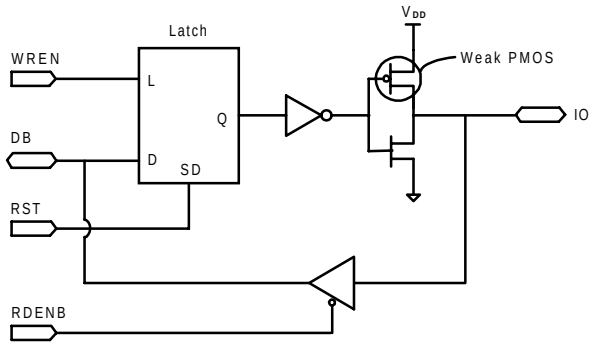


Figure 9.1. I/O Port Structure

10. LED PORT

There are 3 LED direct sink pins which require no external serial resistors. The address is mapped to address $00C9.

Addr.	Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
$00C9	LED	-	-	-	-	-	LED2	LED1	LED0	(W)

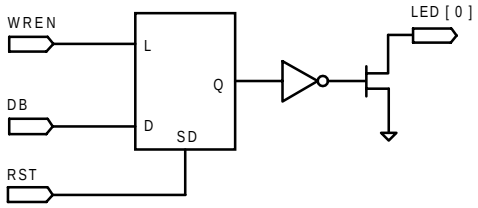


Figure 10.1. LED0 Port Structure

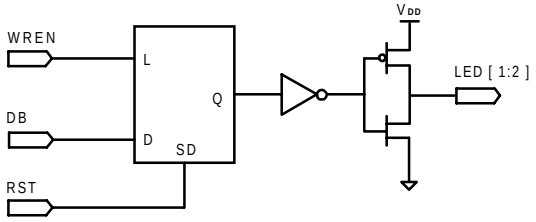


Figure 10.2. LED1, LED2 Port Structures

11. Watch-Dog Timer (WDT)

NT6880 implements a watch-dog timer, which protects programs against system standstill. The clock of the watch-dog timer is derived from the on-chip RC oscillator. The watch-dog timer interval is about 0.175 of a second. The timer must be cleared within every 0.175 second during normal operation; otherwise, it will overflow and cause a system reset. The watch-dog timer is cleared and enabled after a system reset. It cannot be disabled by the software. A user can clear the watch-dog timer by writing #55H to CLRWDT ($00CAH) register.

For example:

```
LDA     #$55
STA     $00CA
```

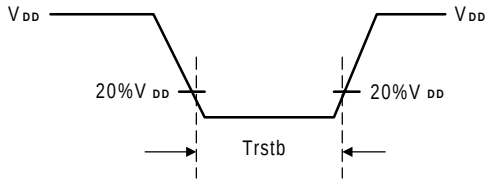
Addr.	Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
$00CA	CLRWDT	0	1	0	1	0	1	0	1	(W)

12. Low Voltage Reset (LVR) Circuit

The NT6880 will check on the voltage level of power supply. When the voltage level of power supply is below a threshold of 3.0V (Typical), the LVRC will issue a reset output to the chip until the power voltage level is above the threshold voltage of 3.0V (Typical) again. As soon as the power voltage arises to 3.0V (Typical), the entire chip will be reset for about 150ms.

13. $\overline{\text{RESET}}$

NT6880 can also be externally reset via the $\overline{\text{RESET}}$ pin. A reset is initiated when the signal at the $\overline{\text{RESET}}$ pin is held Low for at least 10 system clocks. As soon as the $\overline{\text{RESET}}$ signal goes high, the NT6880 begins to be reset for about 150ms. The following shows the definition of the $\overline{\text{RESET}}$ input low pulse width.



Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +7.0V

Input/Output Voltage . . . . . GND -0.2V to V_{DD} + 0.2V

Operating Ambient Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . -55°C to +125°C

Operating Voltage (V_{DD}) . . . . . +4.5V to 5.5V

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

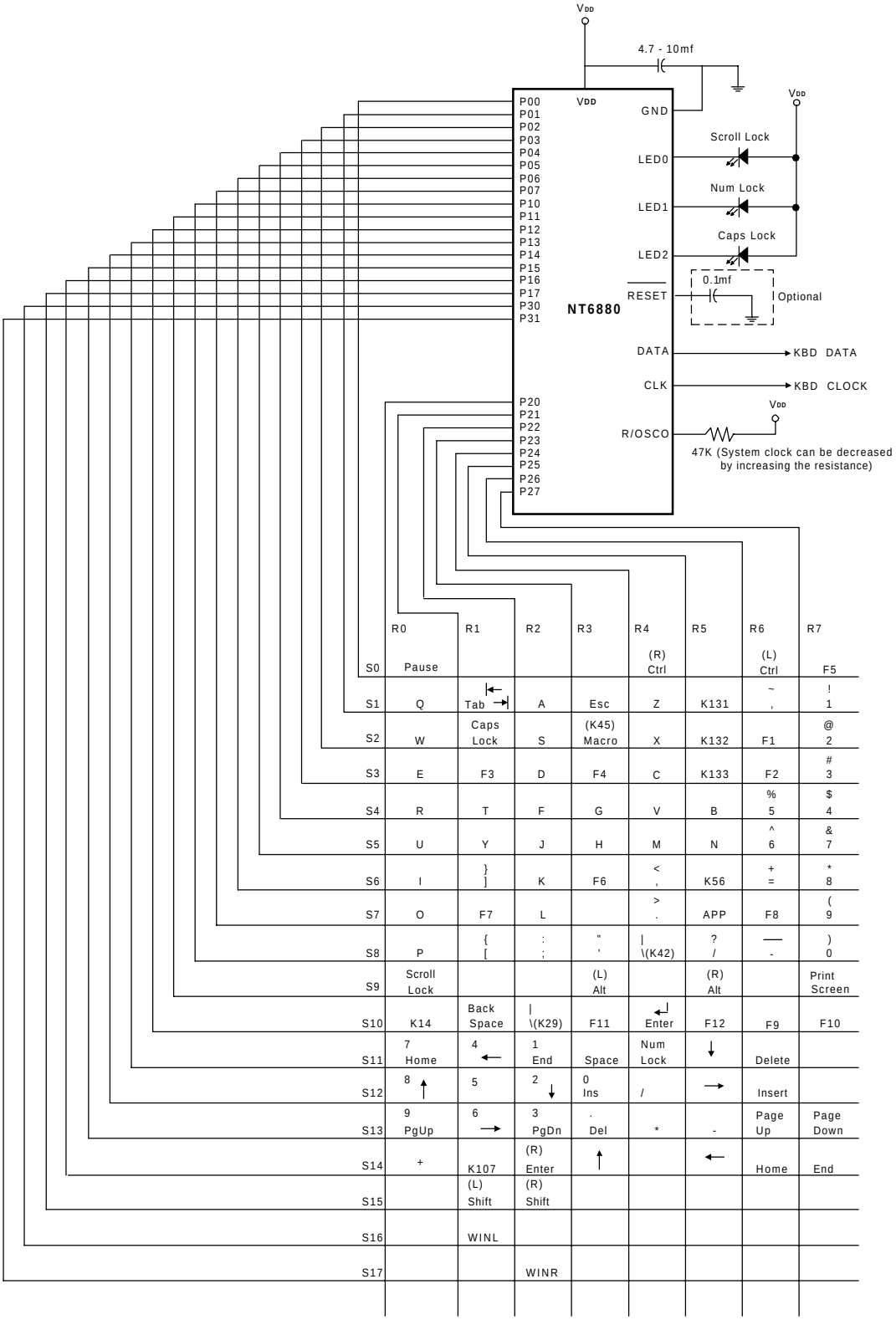
DC Electrical Characteristics (V_{DD} = 5V, GND = 0V, T_A = 25°C, Fosc = 4MHz, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_{CC}	Power Supply Current			20	mA	No load
V_{IH}	Input High Voltage	2			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH1}	Output High Voltage (PORT 0, 1, 2, 3)	2.4			V	I_{OH1} = -100μA
V_{OH2}	Output High Voltage (CLK, DATA)	2.4			V	I_{OH2} = -400μA, *Note 1*
V_{OH3}	Output High Voltage (CLK, DATA)	2.4			V	I_{OH3} = -800μA, *Note 2*
V_{OL1}	Output Low Voltage (PORT 0, 1, 2)			0.4	V	I_{OL1} = 4mA
V_{OL2}	Output Low Voltage (PORT 3)			0.4	V	I_{OL2} = 5mA
V_{OL3}	Output Low Voltage (CLK, DATA)			0.4	V	I_{OL3} = 10mA
ΔF/F	Initial Frequency Variation 1			+/-10	%	For RC OSC option only; by Lots
ΔF/F	Frequency Variation 2			+/-1	%	For ceramic resonator option only; by Lots
I_{LED}	LED Sink Current (LED 0, 1, 2)	10	14	17	mA	V_{OL} = 3.2V
V_{LVR}	Low Voltage Reset Threshold		3.0		V	
T_{POR}	Power-on Reset Time	120	150	180	ms	
T_{RSTB}	$\overline{\text{RESET}}$ Input Low Pulse Width	2.5			μs	10 system clocks
R_{PH}	$\overline{\text{RESET}}$ Pull High Resistor		220		KΩ	

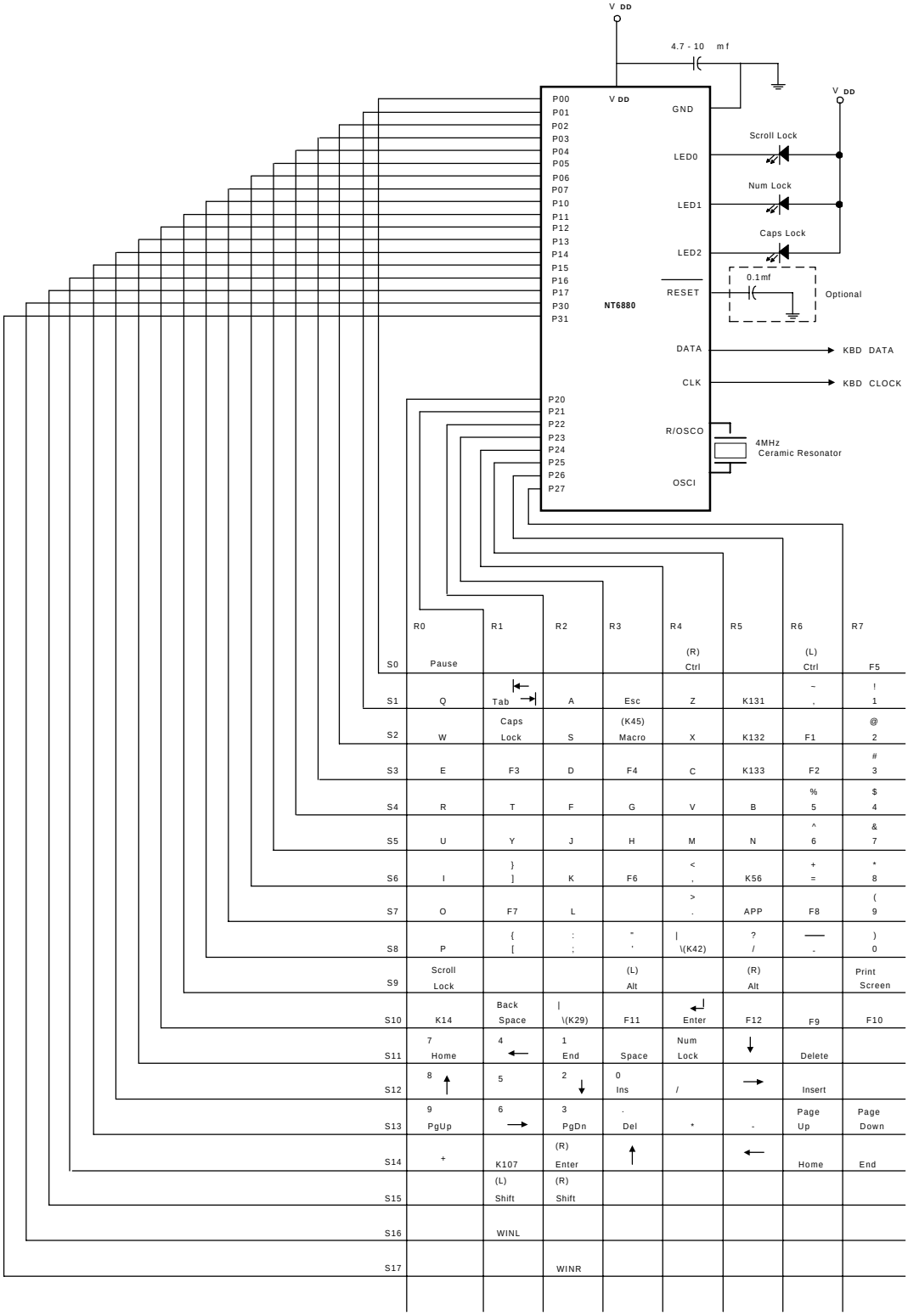
Note 1: There are 2 types for DATA/CLK driving capability. The specification of V_{OH2} is the same as NT6868A. Under this condition, user can select mask option 1 or 3 for this specification.

Note 2: The driving capability of DATA/CLK is higher than V_{OH2}. Under this condition, a user can select mask option 5 or 7 for this specification.

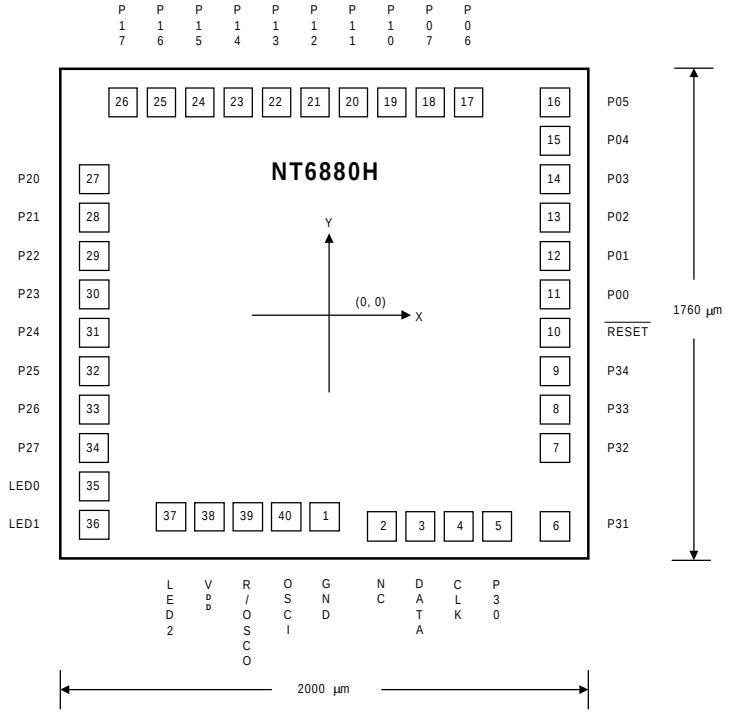
Application Circuit I (for reference only)



Application Circuit II (for reference only)



Bonding Diagram



*Substrate Connect to V_{DD}

unit: µm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	GND	-126.4	-687.1	21	P12	-145.9	752.5
2	NC	3.6	-752.0	22	P13	-275.9	752.5
3	DATA	133.6	-752.0	23	P14	-405.9	752.5
4	CLK	393.6	-752.0	24	P15	-535.9	752.5
5	P30	619.4	-752.0	25	P16	-665.9	752.5
6	P31	865.0	-733.1	26	P17	-808.4	752.5
7	P32	870.2	-435.6	27	P20	-870.2	544.3
8	P33	870.2	-305.6	28	P21	-870.2	414.3
9	P34	870.2	-175.6	29	P22	-870.2	284.3
10	$\overline{\text{RESET}}$	870.2	-45.6	30	P23	-870.2	154.3
11	P00	870.2	84.4	31	P24	-870.2	24.3
12	P01	870.2	214.4	32	P25	-870.2	-105.7
13	P02	870.2	344.4	33	P26	-870.2	-235.7
14	P03	870.2	474.4	34	P27	-870.2	-365.7
15	P04	870.2	604.4	35	LED0	-870.2	-495.7
16	P05	870.2	746.9	36	LED1	-870.2	-641.8
17	P06	374.1	752.5	37	LED2	-646.4	-636.6
18	P07	244.1	752.5	38	V_{DD}	-516.4	-636.6
19	P10	114.1	752.5	39	R/OSCO	-386.4	-636.6
20	P11	-15.9	752.5	40	OSCI	-256.4	-636.6

Ordering Information

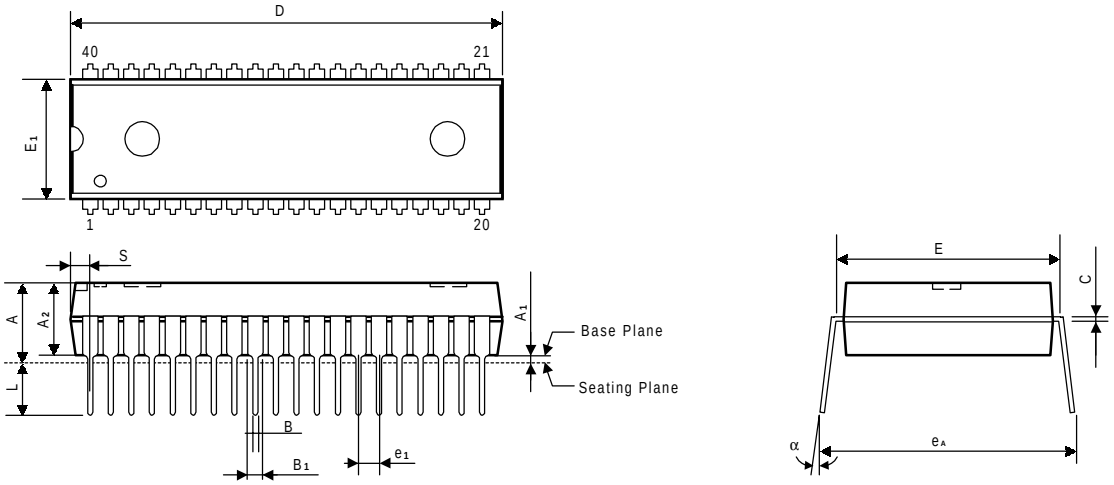
Part No.	Packages
NT6880H	CHIP FORM
NT6880	40L DIP

Code Type No.	Oscillation Type	Data/Clk Driving capacitance
1XXXX	Built-in RC OSC	V_{OH2}
3XXXX	Ceramic Resonator	V_{OH2}
5XXXX	Built-in RC OSC	V_{OH3}
7XXXX	Ceramic Resonator	V_{OH3}

Package Information

DIP 40L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.210 Max.	5.33 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.155±0.010	3.94±0.25
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B_1	0.050 +0.004 -0.002	1.27 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	2.055 Typ. (2.075 Max.)	52.20 Typ. (52.71 Max.)
E	0.600±0.010	15.24±0.25
E_1	0.550 Typ. (0.562 Max.)	13.97 Typ. (14.27 Max.)
e_1	0.100±0.010	2.54±0.25
L	0.130±0.010	3.30±0.25
α	0° ~ 15°	0° ~ 15°
e_A	0.655±0.035	16.64±0.89
S	0.093 Max.	2.36 Max.

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.