

SPICE Device Model Si8417DB Vishay Siliconix

P-Channel 1.8-V (G-S) MOSFET

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

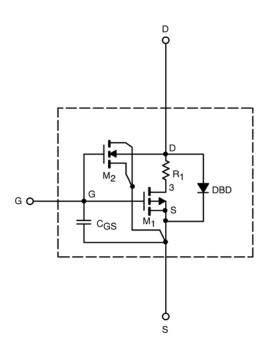
- Apply for both Linear and Switching Application
- Accurate over the –55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

SUBCIRCUIT MODEL SCHEMATIC

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



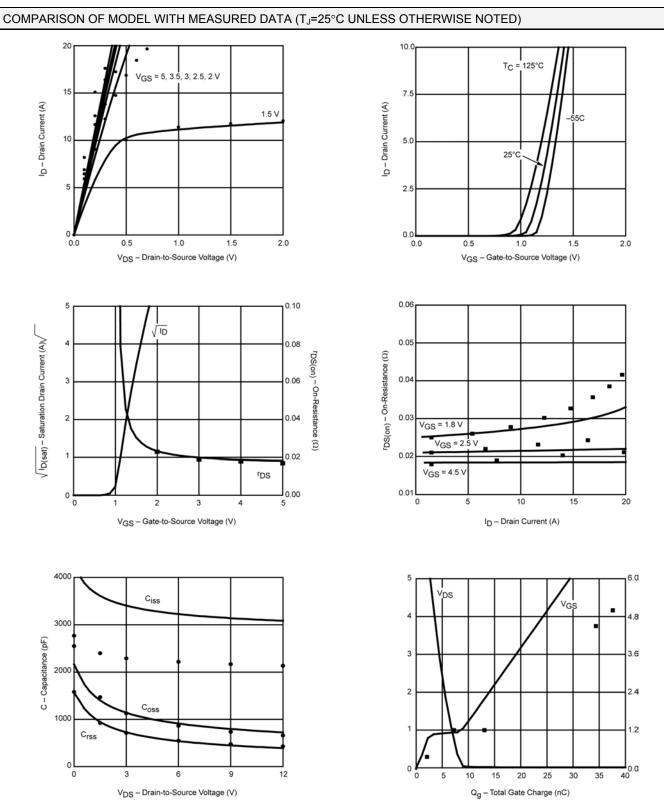
SPECIFICATIONS (TJ = 25°C UN	NLESS OTHERW	ISE NOTED)			
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	V _{GS(th)}	V_{DS} = V_{GS} , I_D = -250 μ A	0.80		V
On-State Drain Current ^a	I _{D(on)}	$V_{\text{DS}} \leq -5V, V_{\text{GS}} = -4.5V$	191		А
Drain-Source On-State Resistance ^a	r _{DS(on)}	$V_{GS} = -4.5V, I_{D} = -1 A$	0.0184	0.0174	Ω
		$V_{GS} = -2.5V, I_D = -1 A$	0.0211	0.0214	
		$V_{GS} = -1.8V, I_D = -1 A$	0.0252	0.0270	
Forward Transconductance ^a	g _{fs}	$V_{DS} = -4V, I_{D} = -1 A$	20	8.3	S
Diode Forward Voltage ^a	V _{SD}	$I_{\rm S}$ = -1A, $V_{\rm GS}$ = 0 V	-0.78	-0.80	V
Dynamic ^b			-		
Input Capacitance	C _{iss}	V_{DS} = -6 V, V_{GS} = 0 V, f = 1 MHz	3228	2220	pF
Output Capacitance	C _{oss}		913	865	
Reverse Transfer Capacitance	C _{rss}		542	555	
Total Gate Charge	Qg	V_{DS} = -6 V, V_{GS} = -5 V, I_{D} = -1 A	25	38	nC
		V_{DS} = -6 V, V_{GS} = -4.5 V, I_D = -1 A	23	35	
Gate-Source Charge	Q _{gs}		7.3	7.3	
Gate-Drain Charge	Q _{gd}		5.9	5.9	

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing.



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Note: Dots and squares represent measured data.