12-Bit, 170/210/250 MSPS 1.8 V A/D Converter

Preliminary Technical Data

AD9230

FEATURES

SNR = 65.5 dBFs @ f_{IN} up to 70 MHz @ 250 MSPS
ENOB of 10.6 @ f_{IN} up to 70 MHz @ 250 MSPS (–0.5 dBFS)
SFDR = 82 dBc@ f_{IN} up to 70 MHz @ 250 MSPS (–0.5 dBFS)
Excellent Linearity
DNL = ±0.3 LSB (Typical)
INL = ±0.5 LSB (Typical)
LVDS at 250 MSPS (ANSI-644 levels)
900 MHz Full Power Analog Bandwidth
On-Chip Reference and Track-and-Hold
Power Dissipation = 425 mW Typical @ 250 MSPS
1.25 V Input Voltage Range
1.8 V Analog Supply Operation
Output Data Format Option
Data Clock Output Provided
Clock Duty Cycle Stabilizer

APPLICATIONS

Wireless and Wired Broadband Communications
Cable Reverse Path
Communications Test Equipment
Radar and Satellite Subsystems
Power Amplifier Linearization

PRODUCT DESCRIPTION

The AD9230 is a 12-bit monolithic sampling analog-to-digital converter optimized for high performance, low power, and ease of use. The product operates up to a 250 MSPS conversion rate and is optimized for outstanding dynamic performance in wideband carrier and broadband systems. All necessary functions, including a track-and-hold (T/H) and voltage reference, are included on the chip to provide a complete signal conversion solution.

The ADC requires a 1.8 V analog voltage supply and a differential clock for full performance operation. The digital outputs are LVDS (ANSI-644) compatible and support either twos complement, offset binary format or gray code. A data clock output is available for proper output data timing.

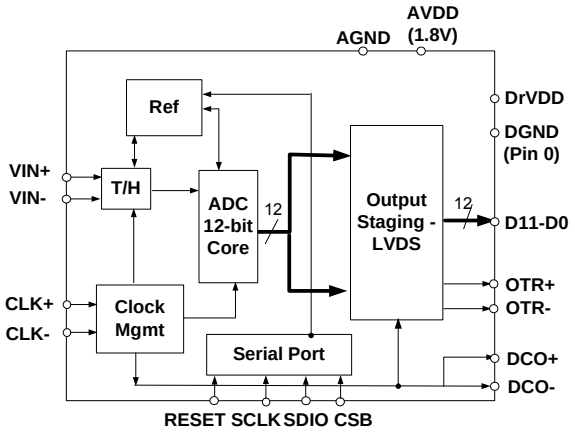

Figure 1. Functional Block Diagram

Fabricated on an advanced CMOS process, the AD9230 is available in a 56-lead chip scale package (56 LFCSP) specified over the industrial temperature range (–40°C to +85°C).

PRODUCT HIGHLIGHTS

1. High Performance—Maintains 65.5 dB SNR @ 250 MSPS with a 65 MHz input.
2. Low Power—Consumes only 425 mW @ 250 MSPS.
3. Ease of Use—LVDS output data and output clock signal allow interface to current FPGA technology. The on-chip reference and sample/hold provide flexibility in system design. Use of a single 1.8 V supply simplifies system power supply design. Supported DDR mode reduces number of output data traces
4. Serial Port Control - Standard serial port interface supports various product functions such as data formatting, enabling a clock duty cycle stabilizer, power down, gain adjust and output test pattern generation.
5. Pin compatible family – 10-bit pin compatible family offered as AD9211.

Rev. PrE

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AD9230–SPECIFICATIONS

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		AD9230-170/-210			AD9230-250			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION			12			12		Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	25°C		TBD			TBD		mV
Gain Error	25°C		TBD			TBD		% FS
Differential Nonlinearity (DNL)	25°C		± 0.3			± 0.3		LSB
	Full		± 0.3			± 0.3		LSB
Integral Nonlinearity (INL)	25°C		± 0.5			± 0.5		LSB
	Full		± 0.5			± 0.5		LSB
TEMPERATURE DRIFT								
Offset Error	Full		TBD			TBD		µV/°C
Gain Error	Full		TBD			TBD		%/°C
ANALOG INPUTS (VIN+, VIN–)								
Differential Input Voltage Range	Full		1.25			1.25		V
Input Common-Mode Voltage	Full		1.3			1.3		V
Input Resistance (differential)	Full		4			4		kΩ
Input Capacitance	25°C		2			2		pF
POWER SUPPLY (LVDS Mode)								
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Currents								
I_{ANALOG}(AVDD = 1.8 V) [1]	Full		150			176		mA
$I_{DIGITAL}$ (DRVDD = 1.8 V)[3]	Full		60			60		mA
Power Dissipation[3]	Full		378			425		mW
Power Supply Rejection	25°C		TBD			TBD		mV/V

[1] I_{AVDD} and I_{DRVDD} are measured with a dc input at rated Clock rate. See Typical Performance Characteristics and Applications sections for I_{ANALOG} and I_{DRVDD} with dynamic input vs clock rate

AC SPECIFICATIONS[1]

Table 2. (AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = –40°C, T_{MAX} = +85°C, f_{IN} = –0.5 dBFS, Internal Reference, Full Scale = 1.25 V, Ain = -0.5dBFS, DCS Enabled unless otherwise noted.)

		AD9230-170/-210			AD9230-250			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SNR								
f_{in}=10 MHz	25°C		65.5			65.5		dB
	Full		65			65		dB
f_{in}=70 MHz	25°C		65.5			65.5		dB
	Full		65			65		dB
f_{in}=100 MHz	25°C		64			64		dB
f_{in}=240 MHz	25°C		63			63		dB
SINAD								
f_{in}=10 MHz	25°C		65			65		dB
	Full		64.8			64.7		dB
f_{in}=70 MHz	25°C		65			65		dB
	Full		64.8			64.7		dB
f_{in}=100 MHz	25°C		63.5			63.5		dB
f_{in}=240 MHz	25°C		62.5			62.5		dB
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{in}=10 MHz	25°C		10.6			10.6		Bits
	Full		10.6			10.6		Bits
f_{in}=70 MHz	25°C		10.6			10.6		Bits
	Full		10.6			10.6		Bits
f_{in}=100 MHz	25°C		10.3			10.3		Bits
f_{in}=240 MHz	25°C		10.2			10.2		Bits
WORST HARMONIC (2nd or 3rd)								
f_{in}=10 MHz	25°C		–82			–82		dBc
	Full		–80			–80		dBc
f_{in}=70 MHz	25°C		–82			–82		dBc
	Full		–80			–80		dBc
f_{in}=100 MHz	25°C		–78			–77		dBc
f_{in}=240 MHz	25°C		–75			–75		dBc
WORST HARMONIC (4^{th} or Higher)								
f_{in}=10 MHz	25°C		–85			–85		dBc
	Full		–85			–85		dBc
f_{in}=70 MHz	25°C		–85			–85		dBc
	Full		–85			–85		dBc
f_{in}=100 MHz	25°C		–83			–83		dBc
f_{in}=240 MHz	25°C		–78			–78		dBc
TWO-TONE IMD[2]								
F1, F2 @ –7 dBFS	25°C		–75			–75		dBc
ANALOG INPUT BANDWIDTH	25°C		900			900		MHz

[1] All ac specifications tested by driving CLK+ and CLK– differentially.
[2] F1 = 28.3 MHz, F2 = 29.3 MHz.

DIGITAL SPECIFICATIONS

Table 3 (AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = –40°C, T_{MAX} = +85°C, DCS Enabled unless otherwise noted.)

		AD9230-170/-210			AD9230-250			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUTS								
Differential Input Voltage[1]	Full	tbd			tbd			V
Common-Mode Voltage[2]	Full		tbd			tbd		V
Input Resistance	Full		tbd			tbd		kΩ
Input Capacitance	25°C		4			4		pF
LOGIC INPUTS								
Logic 1 Voltage	Full	.8 x VDD			2.0			V
Logic 0 Voltage	Full			.2 x AVDD			0.8	V
Logic 1 Input Current	Full			10			10	µA
Logic 0 Input Current	Full			10			10	µA
Input Capacitance	25°C		4			4		pF
LOGIC OUTPUTS[3]								
V_{OD} Differential Output Voltage	Full	247		454	247		454	mV
V_{OS} Output Offset Voltage	Full	1.125		1.375	1.125		1.375	V
Output Coding		Twos Complement,Gray or Binary			Twos Complement,Gray or Binary			

[1] All ac specifications tested by driving CLK+ and CLK– differentially, |(CLK+)– (CLK–)| > 200 mV.
[2] Clock inputs' common mode can be externally set, such that xx.xV < (Clk+ or Clk-) < zzz V.
[3] LVDS $R_{Termination}$ = 100 Ω

SWITCHING SPECIFICATIONS

Table 4. (AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = –40°C, T_{MAX} = +85°C, DCS Enabled unless otherwise noted.)

		AD9230-170/-210			AD9230-250			
Parameter (Conditions)	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Maximum Conversion Rate[1]	Full	170/210			250			MSPS
Minimum Conversion Rate[1]	Full			40			40	MSPS
CLK+ Pulsewidth High (t_{EH})[1]	Full	TBD			TBD			ns
CLK+ Pulsewidth Low (t_{EL})[1]	Full	TBD			TBD			ns
OUTPUT (LVDS)								
Valid Time (t_V)	Full	TBD			TBD			ns
Propagation Delay (t_{PD})	Full		3.9			3.9		ns
Rise Time (t_R) (20% to 80%)	25°C		0.4			0.4		ns
Fall Time (t_F) (20% to 80%)	25°C		0.4			0.4		ns
DCO Propagation Delay (t_{CPD})	Full		3.2			3.2		ns
Data to DCO Skew (t_{PD}– t_{CPD})	Full			TBD			TBD	ns
Latency	Full		5			5		Cycles
Aperture Delay (t_A)	25°C		TBD			TBD		ns
Aperture Uncertainty (Jitter, t_J)	25°C		0.2			0.2		ps rms
Out of Range Recovery Time	25°C			TBD			TBD	Cycles

[1] All ac specifications tested by driving CLK+ and CLK– differentially.

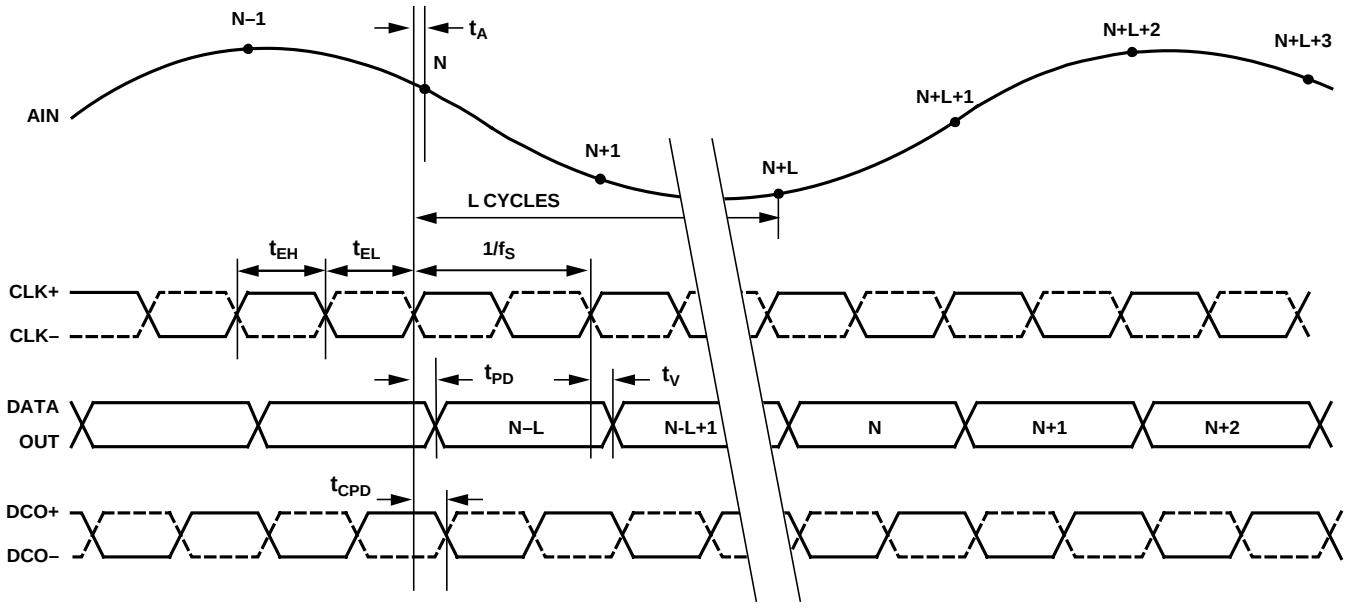

Figure 2. Timing Diagram (L=5 Cycles)

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Rating
AVDD	2.0 V
DRVDD	2.0V
Analog Inputs	–0.5 V to AVDD + 0.5 V
Digital Inputs	–0.5 V to DRVDD + 0.5 V
REFIN Inputs	–0.5 V to AVDD + 0.5 V
Digital Output Current	20 mA
Operating Temperature	–40°C to +125°C
Storage Temperature	–65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C
θ_{JA} [2]	TBD°C/W

1Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

2 Typical θ_{JA} = TBD C/W (heat slug soldered) for multilayer board in still air with solid ground plane.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

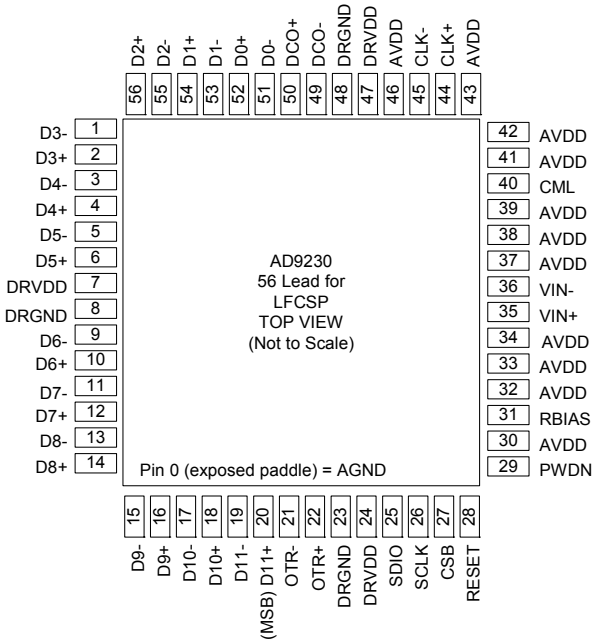

Figure 3. Pinout)

Table 5. PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Description
30,32,33,34,37,38,39,41, 42,43,46	AVDD	1.8 V Analog Supply.
7, 24,47	DRVDD	1.8 V Digital Output Supply.
0	AGND[1]	Analog Ground.
8, 23,48	DRGND[1]	Digital Output Ground.
35	VIN+	Analog Input—True.
36	VIN–	Analog Input—Complement.
40	CML	Analog input common mode output pin
44	CLK+	Clock Input—True.
45	CLK–	Clock Input—Complement.
31	RBIAS	Set Pin for Chip Bias Current. (Place 1% X kohm resistor terminated to ground).
28	RESET	Chip Reset (Active high)
25	SDIO	Serial port input/output pin
26	SCLK	Serial port clock
27	CSB	Serial port chip select (Active low)
29	PWDN	Chip power down
49	DCO–	Data Clock Output—Complement.
50	DCO+	Data Clock Output—True.
51	D0–	D0 Complement Output Bit (LSB).
52	D0+	D0 True Output Bit (LSB).
53	D1–	D1 Complement Output Bit.

[1] AGND and DRGND should be tied to a common quiet ground plane.

Pin Number	Mnemonic	Description
54	D1+	D1 True Output Bit.
55	D2–	D2 Complement Output Bit.
56	D2+	D2 True Output Bit.
1	D3–	D3 Complement Output Bit.
2	D3+	D3 True Output Bit.
3	D4–	D4 Complement Output Bit.
4	D4+	D4 True Output Bit.
5	D5–	D5 Complement Output Bit.
5	D5+	D5 True Output Bit.
9	D6–	D6 Complement Output Bit.
10	D6+	D6 True Output Bit.
11	D7–	D7 Complement Output Bit.
12	D7+	D7 True Output Bit.
13	D8–	D8 Complement Output Bit.
14	D8+	D8 True Output Bit.
15	D9–	D9 Complement Output Bit.
16	D9+	D9 True Output Bit.
17	D10–	D10 Complement Output Bit.
18	D10+	D10 True Output Bit.
19	D11–	D11 Complement Output Bit.
20	D11+	D11 True Output Bit.
21	OTR–	Overrange Complement Output Bit.
22	OTR+	Overrange True Output Bit.

TERMINOLOGY

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay

The delay between the 50% point of the rising edge of the Clock and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Crosstalk

Coupling onto one channel being driven by a low level (–40 dBFS) signal when the adjacent interfering channel is driven by a fullscale signal.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance

The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range

The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180° out of phase. Peak-to-peak differential is computed by rotating the input's phase 180° and again taking the peak measurement. The difference is then computed between both peak measurements.

Differential Nonlinearity

The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)

Calculated from the measured SNR based on the equation

$$ENOB = \frac{SNR_{MEASURED} - 1.76dB}{6.02}$$

Clock Pulsewidth/Duty Cycle

Pulsewidth high is the minimum amount of time the ENCODE pulse should be left in Logic 1 state to achieve rated performance; pulsewidth low is the minimum time the Clock pulse should be left in low state. At a given clock rate, these specifications define an acceptable Clock duty cycle.

Full-Scale Input Power

Expressed in dBm. Computed using the following equation:

$$Power_{FULLSCALE} = 10\log\left(\frac{V^2{}_{FULLSCALE\,RMS}}{\frac{Z_{INPUT}}{0.001}}\right)$$

Gain Error

The difference between the measured and ideal full-scale input voltage range of the ADC.

Harmonic Distortion, Second

The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, Third

The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate

The Clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate

The Clock rate at which parametric testing is performed.

Output Propagation Delay

The delay between a differential crossing of CLK+ and CLK– and the time when all output data bits are within valid logic levels.

Noise (for Any Range within the ADC)

Calculated as follows:

$$V_{NOISE} = \sqrt{Z \times 0.001 \times 10\left(\frac{FS_{dBM} - SNR_{dBc} - Signal_{dBFS}}{10}\right)}$$

where *Z* is the input impedance, *FS* is the full scale of the device for the frequency in question, *SNR* is the value of the particular input level, and *Signal* is the signal level within the ADC

reported in dB below full scale. This value includes both thermal and quantization noise.

Power Supply Rejection Ratio

The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)

The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (without Harmonics)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered) or dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection

The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product; reported in dBc.

Two-Tone SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Worst Other Spur

The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonic) reported in dBc.

Transient Response Time

The time it takes for the ADC to reacquire the analog input after a transient from 10% above negative full scale to 10% below positive full scale.

Out-of-Range Recovery Time

The time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

EQUIVALENT CIRCUITS

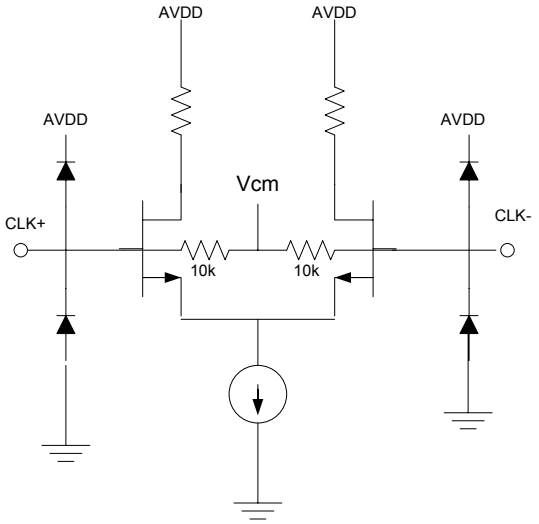

Figure 4 Clock Inputs

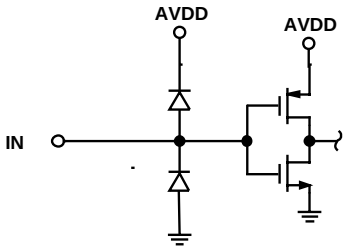

Figure 6. Logic Inputs

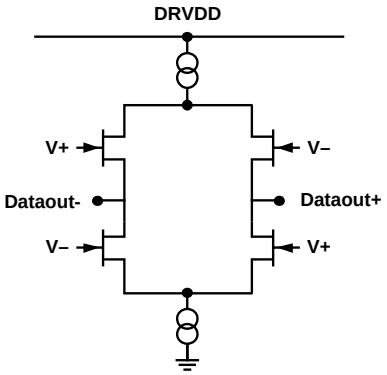

Figure 7. Data Outputs (LVDS Mode)

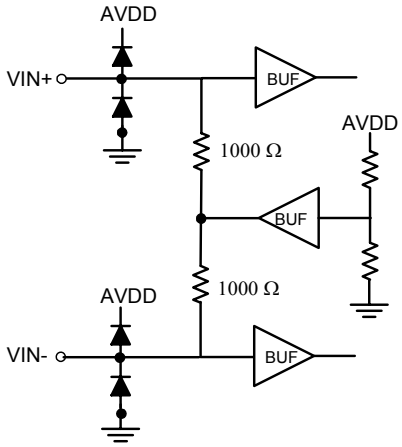

Figure 5. Analog Inputs (VX=~ 1.3V)

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DrVDD = 1.8 V, rated sample rate, , DCS enabled, T_A = 25°C, 1.25 V p-p differential input, AIN = −1dBFS, unless otherwise noted.

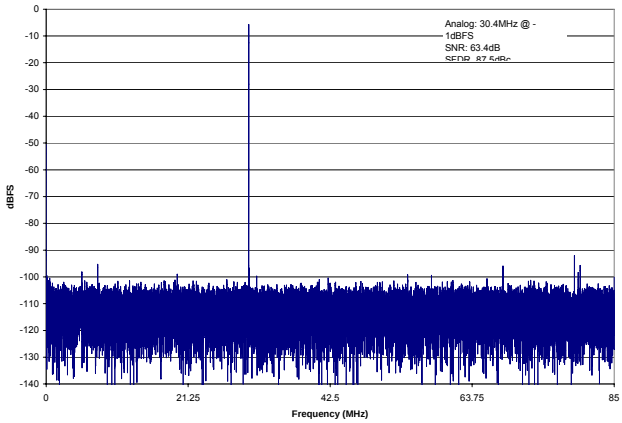

Figure 8. AD9230-170 64k Point Single-Tone FFT/170 MSPS/30.3 MHz

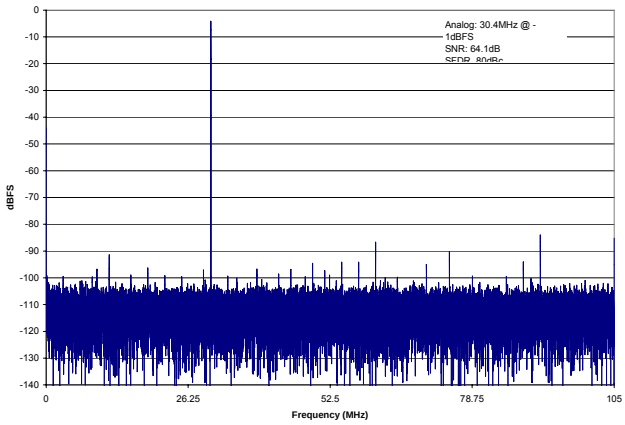

Figure 9. AD9230-210 64k Point Single-Tone FFT/210 MSPS/30.3 MHz

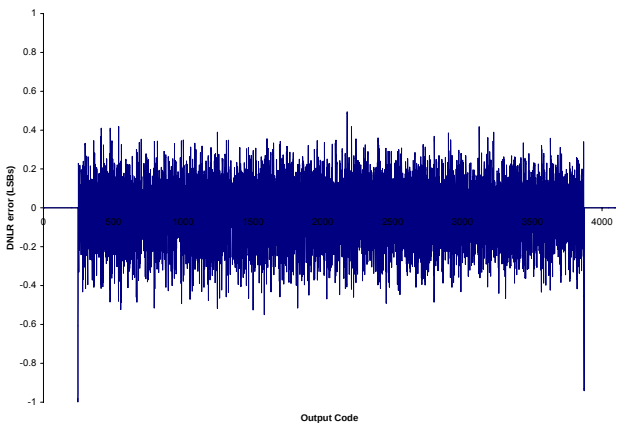

Figure 10. AD9230-250 64k Point Single-Tone FFT/250 MSPS/5.1 MHz z

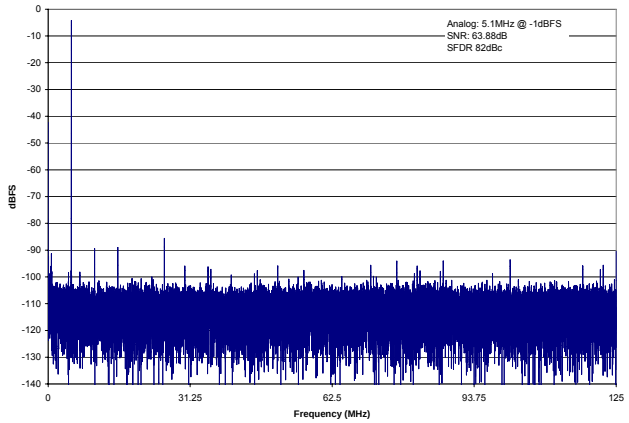

Figure 11. AD9230-250 64k Point Single-Tone FFT/250 MSPS 5.1 MHz

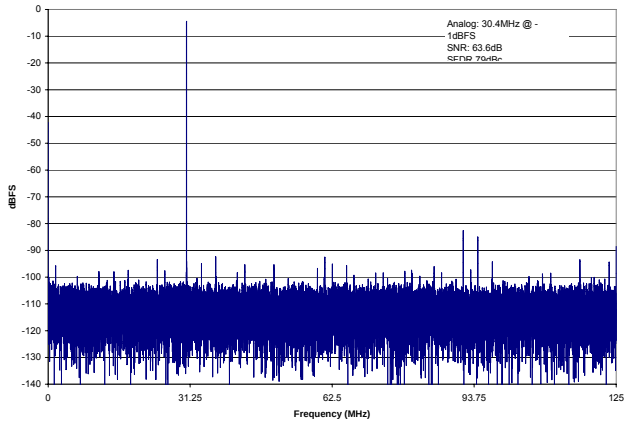

Figure 12. AD9230-250 64k Point Single-Tone FFT/250 MSPS 30.3 MHz

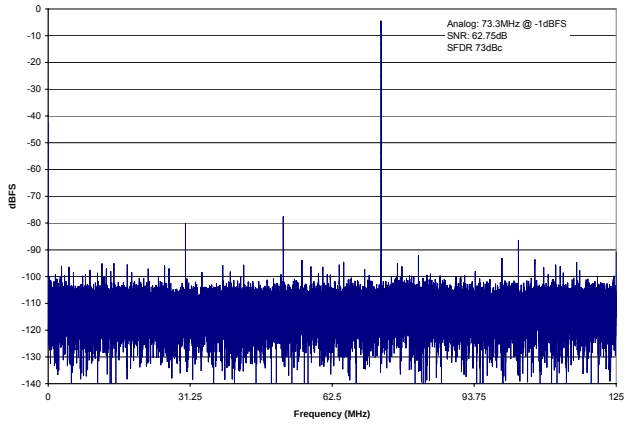

Figure 13. AD9230-250 64k Point Single-Tone FFT/250 MSPS 70.3 MHz

THEORY OF OPERATION

The AD9230 architecture consists of a front-end sample and hold amplifier (SHA) followed by a pipelined switched capacitor ADC. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be ac- or dc-coupled in differential or single-ended modes. The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT AND VOLTAGE REFERENCE

The analog input to the AD9230 is a differential buffer. For best dynamic performance, the source impedances driving VIN+ and VIN– should be matched such that common mode settling errors are symmetrical. The analog input is optimized to provide superior wideband performance and requires that the analog inputs be driven differentially. SNR and SINAD performance degrades significantly if the analog input is driven with a single-ended signal.

A wideband transformer, such as Mini-Circuits' ADT1-1WT, can provide the differential analog inputs for applications that require a single-ended-to-differential conversion. Both analog inputs are self-biased by an on-chip resistor divider to a nominal 1.3 V.

An internal differential voltage reference creates positive and negative reference voltages that define the 1.25Vp-p fixed span of the ADC core. This internal voltage reference can be adjusted by means of SPI control. See SPI control section for more details.

Differential Input Configurations

Optimum performance is achieved while driving the AD9230 in a differential input configuration. For baseband applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the AD8138 is easily set to AVDD/2+0.5V, and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

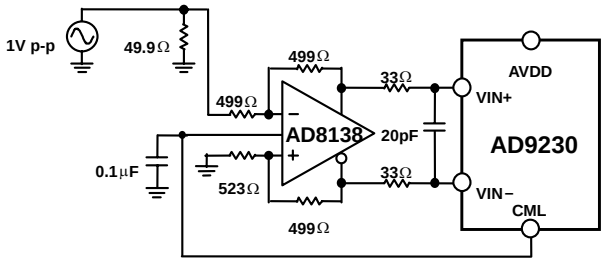

Figure 14. Differential Input Configuration Using the AD8138

At input frequencies in the second Nyquist zone and above, the performance of most amplifiers is not adequate to achieve the true performance of the AD9230. This is especially true in IF under-sampling applications where frequencies in the 70 MHz to 100 MHz range are being sampled. For these applications, differential transformer coupling is the recommended input configuration. The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few MHz, and excessive signal power can also cause core saturation, which leads to distortion.

In any configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

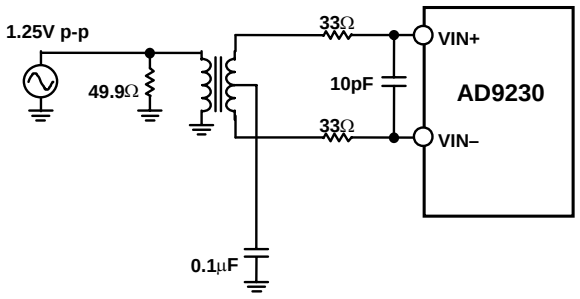

Figure 15. Differential Transformer—Coupled Configuration

Single-Ended Input Configuration

A single-ended input can provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. However, if the source impedances on each input are matched, there should be little effect on SNR performance. Figure 16 details a typical single-ended input configuration.

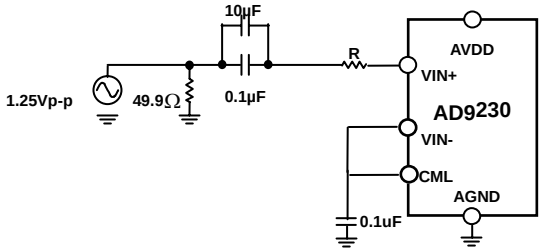

Figure 16. Single-Ended Input Configuration using SPI enabled CML function

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9230 the sample clock inputs (CLK+ and CLK-) should be clocked with a differential signal. This signal is typically ac-coupled into the CLK+ and CLK- pins via a transformer or capacitors. These pins are biased internally and require no additional bias (See Figure X).

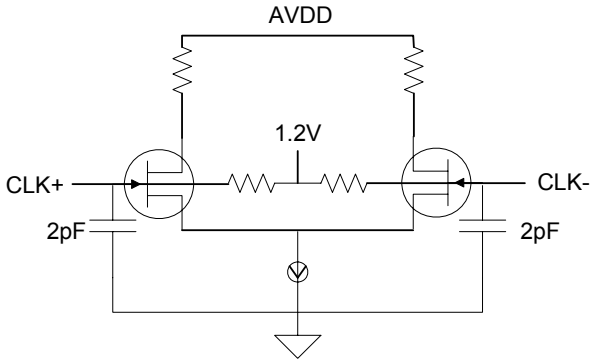

Figure .Equivalent Clock Input Circuit

Figure X shows one preferred method for clocking the AD9230. The clock source (low jitter) is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD9230 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9230 while preserving the fast rise and fall times of the signal, which are critical to a low jitter performance.

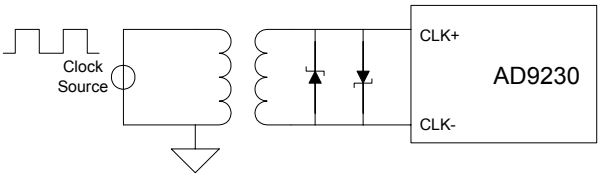

Figure X. Transformer Coupled Differential Clock

If a low jitter clock is available, another option is to ac-couple a differential PECL signal to the sample clock input pins as shown in Figure X. The AD9512 (or same family) from offers excellent jitter performance.

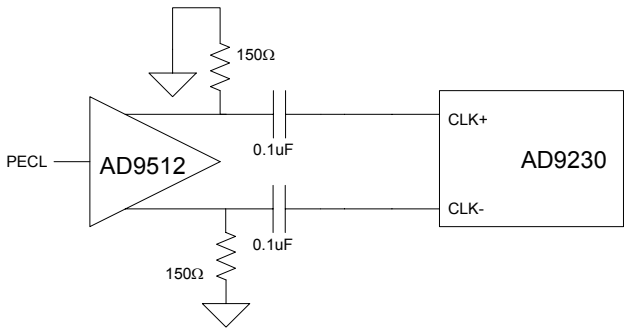

Figure X. Differential PECL Sample Clock

Clock Input Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals, and as a result may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance
characteristics. The AD9230 contains a DCS (duty cycle stabilizer) that retimes the non-sampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9230. Noise and distortion performance are nearly flat for a wide range duty cycles with the DCS on.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the non-sampling edge. As a result, any changes to the sampling frequency require approximately TBD clock cycles to allow the DLL to acquire and lock to the new rate.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{INPUT}) due only to aperture jitter (t_J) can be calculated by

$$\text{SNR} = 20\log\left[\frac{\pi}{2} f_{INPUT} \times t_J\right]$$

In the equation, the rms aperture jitter represents the root-mean square of all jitter sources, which include the clock input, analog input signal, and ADC aperture jitter specification. IF under-sampling applications are particularly sensitive to jitter, see Figure 17.

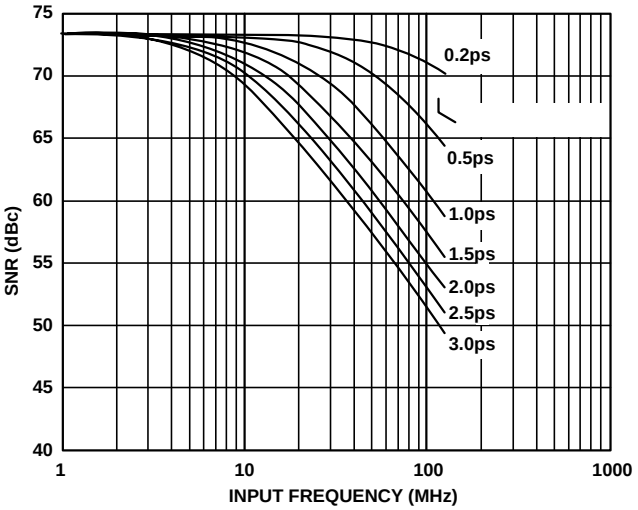

Figure 17. SNR vs. Input Frequency and Jitter

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9230. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

POWER DISSIPATION AND POWER DOWN MODE

As shown in Figure 18 and Figure 20, the power dissipated by the AD9230 is proportional to its sample rate. The digital power dissipation does not vary much because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

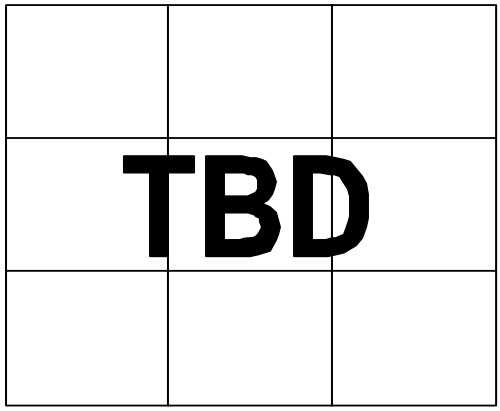

Figure 18. AD9230-170, Supply Current vs. f_{SAMPLE} for f_{IN} = 10.3 MHz

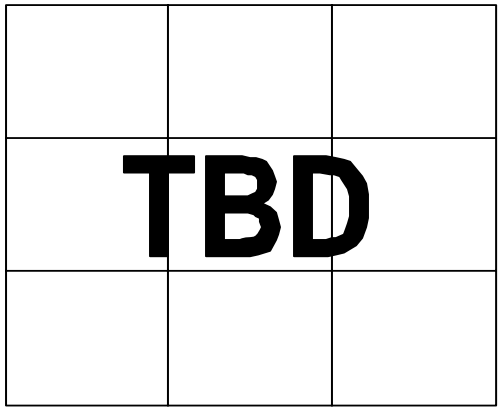

Figure 19. AD9230-210, Supply Current vs. f_{SAMPLE} for f_{IN} = 10.3 MHz

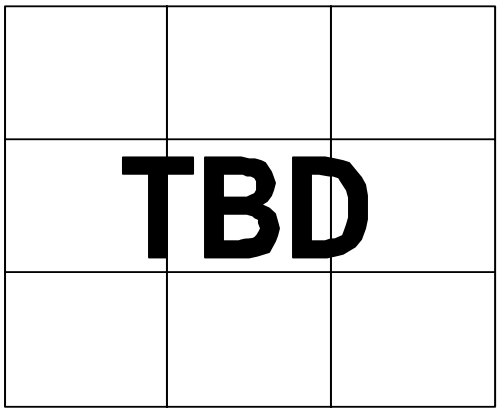

Figure 20. AD9230-250, Supply Current vs. f_{SAMPLE} for f_{IN} = 10.3 MHz

By asserting the PDWN pin high, the AD9230 is placed in standby mode. In this state, the ADC typically dissipates 1 mW even if the CLK and analog inputs are static. During standby, the output drivers are placed in a high impedance state. Reasserting the PDWN pin low returns the AD9230 into its normal operational mode.

An additional stand by mode is supported by means of varying the clock input. When the clock rate falls below 20MHz, the AD9230 will assume a standby state. In this case, the biasing network and internal reference remain on but digital circuitry is powered down. Upon reactivating the clock, the AD9230 will resume normal operation after allowing for the pipeline latency.

DIGITAL OUTPUTS

The AD9228's differential outputs conform to the ANSI-644 LVDS standard on default power up. The LVDS driver current is derived on-chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver.

The AD9230's LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close to the receiver as possible. It is recommended to keep the trace length no longer than 12 inches and to keep differential output traces close together and at equal lengths.

The format of the output data is offset binary. An example of the output coding format can be found in Table 7.

Table 7. Digital Output Coding

Code	(VIN+) – (VIN–), Input Span = 1.252 V p-p (V)	Digital Output Offset Binary (D11 ... D0)
4095	1.000	1111 1111 1111
2048	0	1000 0000 0000
2047	−0.000488	0111 1111 1111
0	−1.00	0000 0000 0000

As detailed in *Interfacing to ADC SPI*, the data format can be selected for either offset binary or twos complement, or Gray code (SPI access only).

Out-of-Range (OTR)

An out-of-range condition exists when the analog input voltage is beyond the input range of the ADC. OTR is a digital output that is updated along with the data output corresponding to the particular sampled input voltage. Thus, OTR has the same pipeline latency as the digital data. OTR is low when the analog input voltage is within the analog input range and high when the analog input voltage exceeds the input range as shown in Figure 21. OTR will remain high until the analog input returns to within the input range and another conversion is completed. By logically AND-ing OTR with the MSB and its complement, over-range high or under-range low conditions can be detected.

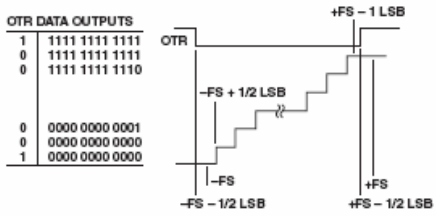

Figure 12. OTR Relation to Input Voltage and Output Data

Figure 21. OTR Relation to Input Voltage and Output Data

TIMING

The AD9230 provides latched data outputs with a pipeline delay of five clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9230. These transients can degrade the converter's dynamic performance. The AD9230 also provides data clock output (DCO) intended for capturing the data in an external register. The data outputs are valid on the rising edge of DCO.

The lowest typical conversion rate of the AD9230 is 40 MSPS. At clock rates below 1 MSPS, the AD9230 will assume standby mode.

RBIAS

The AD9230 requires the user to place a 10KΩ resistor between the RBIAS pin and ground. This resister should have a 1% tolerance, and is used to set the master current reference of the ADC core.

AD9230 CONFIGURATION USING THE SPI

The AD9230 serial port interface allows the user to configure the converter for specific functions or operations through a structured register space inside the ADC. This gives the user added flexibility to customize device operation depending on the application. Addresses are accessed (programmed or read back) serially in one-byte words. Each byte may be further divided down into fields which are documented in the Memory Map Section below.

There are three pins that define the serial port interface or SPI to this particular ADC. They are the SPI SCLK / DFS, SPI SDIO / DCS, and CSB pins. The SCLK/DFS (serial clock) is used to synchronize the read and write data presented the ADC.. The SDIO / DCS (serial data input/output) is a dual purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB or chip select bar is an active low control that enables or disables the read and write cycles. See Table X.

Table X. Serial Port Pins

Pin	Function
SCLK	SCLK (Serial Clock) is the serial shift clock in. SCLK is used to synchronize serial interface reads and writes.
SDIO	SDIO (Serial Data Input/Output) is a dual purpose pin. The typical role for this pin is an input and output depending on the instruction being sent and the relative position in the timing frame.
CSB	CSB (Chip Select Bar) is active low controls that gates the read and write cycles.
RESET	Master device reset. When asserted, device assumes default settings.

The falling edge of the CSB in conjunction with the rising edge of the SCLK determines the start of the framing. An example of the serial timing and its definitions can be found in Figure X and Table X. Table X. SPI Timing Diagram specifications

Spec Name	Meaning
t_{DS}	Setup time between data and rising edge of SCLK
t_{DH}	Hold time between data and rising edge of SCLK
t_{CLK}	Period of the clock
t_S	Setup time between CSB and SCLK
t_H	Hold time between CSB and SCLK
t_{HI}	Minimum period that SCLK should be in a logic high state
t_{LO}	Minimum period that SCLK should be in a logic low state

During an instruction phase a 16bit instruction is transmitted. Data then follows the instruction phase and is determined by the W0 and W1 bits which is 1 or more bytes of data. All data is composed of 8bit words. The first bit of each individual byte of serial data indicates whether this is a read or write command. This allows the serial data input/output (SDIO) pin to change direction from an input to an output.

Data may be sent in MSB or in LSB first mode. MSB first is default on power up and may be changed by changing the configuration register. For more information about this feature and others see SPI Doc at www.analog.com.

HARDWARE INTERFACE

The pins described in Table X comprise the physical interface between the user's programming device and the serial port of the AD9230. All serial pins are inputs, which is an open-drain output and should be tied to an external pull-up or pull-down resistor (suggested value 10 kΩ).

This interface is flexible enough to be controlled by either PROMS or PIC mirocontrollers as well. This provides the user to use an alternate method to program the ADC other than a SPI controller.

If the user chooses to not use the SPI interface, some pins serve a dual function and are associated with a specific function when strapped externally to AVDD or ground during device power on. The section below describes the strappable functions supported on the AD9230. AD9230

CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SPI SDIO / DCS and SPI SCLK / DFS pins can alternately serve as stand alone CMOS compatible control pins When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the duty cycle stabilizer. In this mode the SPI CSB chip select should be connected to AVDD, which will disable the serial port interface.

Table 6. Mode Selection

Pin	External Voltage	Configuration
SPI SDIO / DCS	AVDD	Duty Cycle Stabilizer Enabled
	AGND	Duty Cycle Stabilizer Disabled
SPI SCLK / DFS	AVDD	2's Complement Enabled
	AGND	Offset Binary Enabled

READING THE MEMORY MAP TABLE

Each row in the memory map table has eight address locations. The memory map is roughly divided into four sections: chip configuration register map (Address 0x00 to Address 0x02), device index and transfer register map (Address 0x04 to Address 0x05, and Address 0xFF), global ADC function register map (Address 0x08 to Address 0x09), and flexible ADC functions register map (Address 0x0B to Address 0x25). The flexible ADC functions register map is product specific.

Starting from the right hand column, the memory map register in Table X documents the default hex value for each hex address shown. The column with the heading Byte 7 (MSB) is the start of the default hex value giving. For example, hex address 0x14, flex_output_phase has a hex default value of 00h. This means Bit 3 = 0, Bit 2 = 0, Bit 1 = 1, and Bit 0 = 1 or 0011 in binary. This setting is the default output clock or DCO phase adjust option. The default value adjusts the DCO phase 90deg relative to the Nominal DCO edge and 180deg relative to the data edge. For more information on this function and others consult the SPI Doc at www.analog.com.

OPEN LOCATIONS

All locations marked as "open" are currently not supported for this particular device. When required, these locations should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x14). If the whole address location is open (for example, Address 0x13), then this address location does not need to be written.

DEFAULT VALUES

Coming out of reset, some of the address locations (but not all) are loaded with default values. The default values for the registers are given in the Table X.

LOGIC LEVELS

An explanation of various registers, "bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit." Similarly "clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

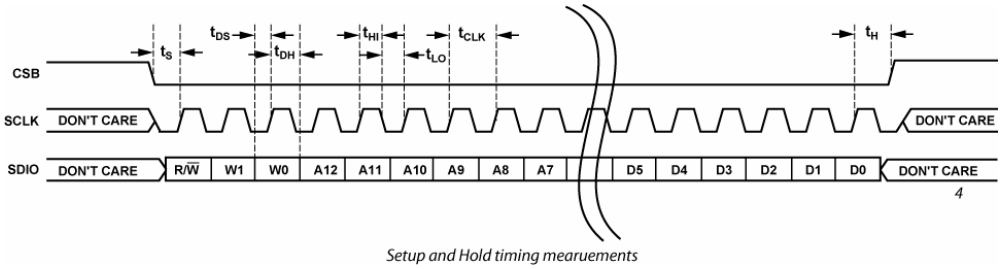

Figure X. Serial Port Interface Timing Diagram

Table X. AD9230 Device Configuration Register Memory Map

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OUTLINE DIMENSIONS

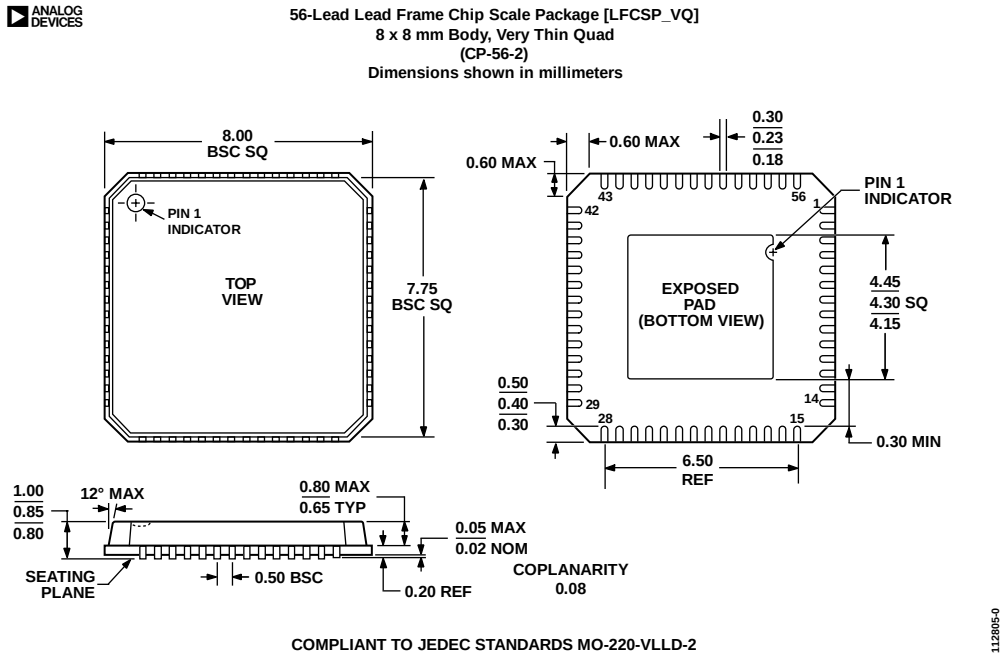

Figure 22. Mechanical Drawing (Subject to change)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9230BCPZ-170[1]	−40°C to +85°C	56-Lead Lead Frame Chip Scale Package (LFCSP-VQ)	CP-56
AD9230BCPZ-210[1]	−40°C to +85°C	56-Lead Lead Frame Chip Scale Package (LFCSP-VQ)	CP-56
AD9230BCPZ-250[1]	−40°C to +85°C	56-Lead Lead Frame Chip Scale Package (LFCSP-VQ)	CP-56
AD9230-250EB	25°C	LVDS Evaluation Board with AD9230BCPZ-250	
AD9230-210EB	25°C	LVDS Evaluation Board with AD9230BCPZ-210	
AD9230-170EB	25°C	LVDS Evaluation Board with AD9230BCPZ-170	

[1] Z=Pb-free part