



# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

MAX14800-MAX14803

## General Description

The MAX14800–MAX14803 provide high-voltage switching on 16 channels for ultrasonic imaging and printer applications. The devices utilize HVCMOS process technology to provide 16 high-voltage low-charge-injection SPST switches, controlled by a digital interface. Data is clocked into an internal 16-bit shift register and retained by a programmable latch with enable and clear inputs. A power-on reset function ensures that all switches are open on power-up.

The MAX14800–MAX14803 operate with a wide range of high-voltage supplies including:  $V_{PP}/V_{NN} = +100V/-100V$ ,  $+200V/0V$ , and  $+40V/-160V$ . The digital interface operates from a separate  $+2.7V$  to  $+5.5V$   $V_{DD}$  supply. Digital inputs DIN, CLK,  $\overline{LE}$ , and CLR operate on the  $V_{DD}$  supply voltage.

The MAX14801/MAX14803 provide integrated  $35k\Omega$  bleed resistors on each switch terminal to discharge capacitive loads. The MAX14802/MAX14803 provide integrated clamping diodes for overvoltage protection against positive overshoot.

The MAX14800–MAX14803 are available in the 48-pin TQFP package. All devices are specified for the commercial  $0^{\circ}C$  to  $+70^{\circ}C$  temperature range.

## Applications

Ultrasound Imaging  
Printers

## Features

- ◆ Integrated Overvoltage Protection (MAX14802/MAX14803)
- ◆ 20MHz Serial Interface (5V)
- ◆ HVCMOS Technology for High Performance
- ◆ Individually Programmable High-Voltage Analog Switches
- ◆ Very Low  $5\mu A$  (typ) Quiescent Current
- ◆ DC-to-20MHz Low-Voltage Analog Signal Frequency Range
- ◆ 2.7V to 5.5V Logic Supply Voltage
- ◆ Low-Charge Injection, Low-Capacitance  $R_L$  Switches
- ◆ -77dB (typ) Off-Isolation at 5MHz ( $R_L = 50\Omega$ )
- ◆ Daisy-Chainable Serial Interface
- ◆ Flexible High-Voltage Supplies ( $V_{PP} - V_{NN} = 250V$ )

*Pin Configuration appears at end of data sheet.*

## Ordering Information/Selector Guide

| PART          | SWITCH CHANNELS | BLEED RESISTOR | OVP | SECOND SOURCE | PIN-PACKAGE | TEMP RANGE                     |
|---------------|-----------------|----------------|-----|---------------|-------------|--------------------------------|
| MAX14800CCM+* | 16              | No             | No  | HV2601        | 48 TQFP     | $0^{\circ}C$ to $+70^{\circ}C$ |
| MAX14801CCM+* | 16              | Yes            | No  | HV2701        | 48 TQFP     | $0^{\circ}C$ to $+70^{\circ}C$ |
| MAX14802CCM+  | 16              | No             | Yes | —             | 48 TQFP     | $0^{\circ}C$ to $+70^{\circ}C$ |
| MAX14803CCM+  | 16              | Yes            | Yes | —             | 48 TQFP     | $0^{\circ}C$ to $+70^{\circ}C$ |

+Denotes a lead(Pb)-free/RoHS-compliant package.

\*Future product—contact factory for availability.

Parts with extended temperature range ( $-40^{\circ}C$  to  $+85^{\circ}C$ ) are available upon request.

# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

## ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

|   |  |
|---|--|
| V <sub>DD</sub> Logic-Supply Voltage                      | -0.3V to +7V   |
| V <sub>PP</sub> - V <sub>NN</sub> Supply Voltage          | 260V   |
| V <sub>PP</sub> Positive-Supply Voltage                   | -0.3V to +220V   |
| V <sub>NN</sub> Negative-Supply Voltage                   | -0.3V to -220V   |
| Logic Inputs (LE, CLR, CLK, DIN, DOUT)                    | -0.3V to +7V   |
| COM <sub>_</sub> , NO <sub>_</sub><br>(MAX14800/MAX14801) | (-0.3V + V <sub>NN</sub> ) to (V <sub>NN</sub> + 220V)   |
| COM <sub>_</sub> , NO <sub>_</sub><br>(MAX14802/MAX14803) | (-0.3V + V <sub>NN</sub> ) to the minimum of<br>[(V <sub>NN</sub> + 220V) or (V <sub>PP</sub> + 0.3V)] |

|  |                 |
|--|-----------------|
| Peak Analog Signal Current Per Channel                             | 3A              |
| Continuous Power Dissipation (T <sub>A</sub> = +70°C)              |                 |
| 48-Pin TQFP (derate 22.7mW/°C above +70°C)                         | 1818mW          |
| Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ) (Note 1) |                 |
| 48-Pin TQFP  | 44°C/W          |
| Junction-to-Case Thermal Resistance (θ <sub>JC</sub> ) (Note 1)    |                 |
| 48-Pin TQFP  | 10°C/W          |
| Operating Temperature Range  | 0°C to +70°C    |
| Storage Temperature Range  | -65°C to +150°C |
| Junction Temperature   | +150°C          |
| Lead Temperature (soldering, 10s)                                  | +300°C          |

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maxim-ic.com/thermal-tutorial](http://www.maxim-ic.com/thermal-tutorial).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +2.7V to +5.5V, V<sub>PP</sub> = +40V to V<sub>NN</sub> + 250V, V<sub>NN</sub> = -40V to -160V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 2)

| PARAMETER   | SYMBOL                               | CONDITIONS  | MIN             | TYP  | MAX  | UNITS |
|---|--------------------------------------|---|-----------------|------|--|-------|
| <b>POWER SUPPLIES</b>   |                                      |   |                 |      |  |       |
| V <sub>DD</sub> Supply Voltage  | V <sub>DD</sub>                      |   | +2.7            |      | +5.5   | V     |
| V <sub>PP</sub> Supply Voltage  | V <sub>PP</sub>                      |   | +40             | +100 | V <sub>NN</sub> + 250                                      | V     |
| V <sub>NN</sub> Supply Voltage  | V <sub>NN</sub>                      |   | -160            | -100 | 0  | V     |
| V <sub>DD</sub> Supply Quiescent Current                                      | I <sub>DDQ</sub>                     |   |                 |      | 5  | μA    |
| V <sub>DD</sub> Supply Dynamic Current  | I <sub>DD</sub>                      | V <sub>DD</sub> = +5V, LE = +5V, f <sub>CLK</sub> = 5MHz                    |                 |      | 0.5  | mA    |
| V <sub>PP</sub> Supply Quiescent Current                                      | I <sub>PPQ</sub>                     | All switches remain on or off, I <sub>COM_</sub> = 5mA                      |                 | 0    | 10   | μA    |
| V <sub>PP</sub> Supply Dynamic Current (All Channel Switching Simultaneously) | I <sub>PP</sub>                      | V <sub>PP</sub> = +40V, V <sub>NN</sub> = -160V, f <sub>COM_</sub> = 50kHz  |                 |      | 4  | mA    |
|   |                                      | V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V, f <sub>COM_</sub> = 50kHz |                 | 3.4  | 6  |       |
|   |                                      | V <sub>PP</sub> = +160V, V <sub>NN</sub> = -40V, f <sub>COM_</sub> = 50kHz  |                 |      | 8  |       |
| V <sub>NN</sub> Supply Quiescent Current                                      | I <sub>NNQ</sub>                     | All switches remain on or off, I <sub>COM_</sub> = 5mA                      |                 | 0    | 10   | μA    |
| V <sub>NN</sub> Supply Dynamic Current (All Channel Switching Simultaneously) | I <sub>NN</sub>                      | V <sub>PP</sub> = +40V, V <sub>NN</sub> = -160V, f <sub>COM_</sub> = 50kHz  |                 |      | 5  | mA    |
|   |                                      | V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V, f <sub>COM_</sub> = 50kHz |                 | 2.3  | 4  |       |
|   |                                      | V <sub>PP</sub> = +160V, V <sub>NN</sub> = -40V, f <sub>COM_</sub> = 50kHz  |                 |      | 3  |       |
| <b>ANALOG SWITCH</b>  |                                      |   |                 |      |  |       |
| COM <sub>_</sub> , NO <sub>_</sub> Analog Signal Range                        | V <sub>COM_</sub> , V <sub>NO_</sub> | (Note 3)  | V <sub>NN</sub> |      | min of (V <sub>NN</sub> + 200V) or (V <sub>PP</sub> - 10V) | V     |

# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

MAX14800-MAX14803

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +2.7V$  to  $+5.5V$ ,  $V_{PP} = +40V$  to  $V_{NN} + 250V$ ,  $V_{NN} = -40V$  to  $-160V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 2)

| PARAMETER   | SYMBOL                                | CONDITIONS   | MIN                 | TYP | MAX  | UNITS      |
|---|---------------------------------------|--|---------------------|-----|------|------------|
| Small-Signal Switch On-Resistance                   | RONS                                  | $V_{PP} = +40V$ , $V_{NN} = -160V$ ,<br>$V_{COM\_} = 0$                      | $I_{COM\_} = 5mA$   | 26  | 48   | $\Omega$   |
|   |                                       |  | $I_{COM\_} = 200mA$ | 22  | 32   |            |
|   |                                       | $V_{PP} = +100V$ , $V_{NN} = -100V$ ,<br>$V_{COM\_} = 0$                     | $I_{COM\_} = 5mA$   | 22  | 30   |            |
|   |                                       |  | $I_{COM\_} = 200mA$ | 18  | 27   |            |
|   |                                       | $V_{PP} = +160V$ , $V_{NN} = -40V$ ,<br>$V_{COM\_} = 0$                      | $I_{COM\_} = 5mA$   | 20  | 30   |            |
|   |                                       |  | $I_{COM\_} = 200mA$ | 16  | 27   |            |
| Small-Signal Switch On-Resistance Matching          | $\Delta RONS$                         | $V_{PP} = +100V$ , $V_{NN} = -100V$ , $V_{COM\_} = 0$ ,<br>$I_{COM\_} = 5mA$ |                     | 5   |      | %          |
| Large-Signal Switch On-Resistance                   | RONL                                  | $V_{COM\_} = V_{PP} - 10V$ , $I_{COM\_} = 1A$                                |                     | 15  |      | $\Omega$   |
| Shunt Resistance                                    | $R_{INT}$                             | NO_ or COM_ to GND<br>(MAX14801/MAX14803), switch off                        | 30                  | 40  | 50   | k $\Omega$ |
| Switch-Off Leakage                                  | $I_{COM\_}(OFF)$ ,<br>$I_{NO\_}(OFF)$ | $V_{COM\_}$ , $V_{NO\_} = +100V$ or unconnected                              |                     | 0   | 2    | $\mu A$    |
| Switch-Off DC Offset                                |                                       | $R_L = 100k\Omega$   | -30                 |     | +30  | mV         |
| Switch-Output Peak Current (Note 4)                 |                                       | 100ns pulse width, 0.1% duty cycle   |                     | 3   |      | A          |
| Switch-Output COM_ Isolation Diode Current (Note 4) |                                       | 300ns pulse width, 2% duty cycle<br>(MAX14802/MAX14803)                      |                     | 500 |      | mA         |
| <b>SWITCH DYNAMIC CHARACTERISTICS</b>               |                                       |  |                     |     |      |            |
| Turn-On Time  | $t_{ON}$                              | $V_{NO\_} = +100V$ , $R_L = 10k\Omega$ ,<br>$V_{NN} = -100V$                 |                     | 2   | 3.5  | $\mu s$    |
| Turn-Off Time                                       | $t_{OFF}$                             | $V_{NO\_} = +100V$ , $R_L = 10k\Omega$ ,<br>$V_{NN} = -100V$                 |                     | 2   | 3.5  | $\mu s$    |
| Output Switching Frequency                          | $f_{SW}$                              | Duty cycle = 50%   |                     |     | 50   | kHz        |
| Maximum $V_{COM\_}$ , $V_{NO\_}$ Slew Rate          | $dV/dt$                               | (Note 4)   | 20                  |     |      | V/ns       |
| Off-Isolation                                       | $V_{ISO}$                             | $f = 5MHz$ , $R_L = 1k\Omega$ , $C_L = 15pF$                                 |                     | -50 |      | dB         |
|   |                                       | $f = 5MHz$ , $R_L = 50\Omega$  |                     | -77 |      |            |
| Crosstalk   | $V_{CT}$                              | $f = 5MHz$ , $R_L = 50\Omega$  |                     | -80 |      | dB         |
| COM_ NO_ Off-Capacitance (Note 4)                   | $C_{COM\_}(OFF)$ ,<br>$C_{NO\_}(OFF)$ | $V_{COM\_} = 0$ , $V_{NO\_} = 0$ , $f = 1MHz$                                | 4                   | 11  | 18   | pF         |
| COM_ On-Capacitance (Note 4)                        | $C_{COM\_}(ON)$                       | $V_{COM\_} = 0$ , $f = 1MHz$   | 20                  | 36  | 56   | pF         |
| Output-Voltage Spike (Note 4)                       | $V_{SPK}$                             | $R_L = 50\Omega$   | -150                |     | +150 | mV         |
| Small-Signal Analog Bandwidth                       | $f_{BW}$                              | $V_{PP} = +100V$ , $V_{NN} = -100V$ , $C_L = 200pF$                          |                     | 20  |      | MHz        |

# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +2.7V$  to  $+5.5V$ ,  $V_{PP} = +40V$  to  $V_{NN} + 250V$ ,  $V_{NN} = -40V$  to  $-160V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 2)

| PARAMETER                        | SYMBOL   | CONDITIONS  | MIN             | TYP | MAX  | UNITS   |
|----------------------------------|----------|---|-----------------|-----|------|---------|
| Charge Injection                 | Q        | $V_{PP} = +40V$ , $V_{NN} = -160V$ , $V_{COM\_} = 0$  |                 | 820 |      | pC      |
|                                  |          | $V_{PP} = +100V$ , $V_{NN} = -100V$ , $V_{COM\_} = 0$ |                 | 600 |      |         |
|                                  |          | $V_{PP} = +160V$ , $V_{NN} = -40V$ , $V_{COM\_} = 0$  |                 | 350 |      |         |
| <b>LOGIC LEVELS</b>              |          |   |                 |     |      |         |
| Logic-Input Low Voltage          | $V_{IL}$ |   |                 |     | 0.75 | V       |
| Logic-Input High Voltage         | $V_{IH}$ |   | $V_{DD} - 0.75$ |     |      | V       |
| Logic-Output Low Voltage         | $V_{OL}$ | $I_{SINK} = 1mA$                                      |                 |     | 0.4  | V       |
| Logic-Output High Voltage        | $V_{OH}$ | $I_{SOURCE} = 0.75mA$                                 | $V_{DD} - 0.5$  |     |      | V       |
| Logic-Input Capacitance (Note 4) | $C_{IN}$ |   |                 |     | 10   | pF      |
| Logic-Input Leakage              | $I_{IN}$ |   | -1              |     | +1   | $\mu A$ |

## TIMING CHARACTERISTICS

( $V_{DD} = +2.7V$  to  $+5.5V$ ,  $V_{PP} = +40V$  to  $V_{NN} + 200V$ ,  $V_{NN} = -40V$  to  $-160V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 2)

| PARAMETER                         | SYMBOL     | CONDITIONS              | MIN | TYP | MAX | UNITS |
|-----------------------------------|------------|-------------------------|-----|-----|-----|-------|
| <b>LOGIC TIMING (Figure 1)</b>    |            |                         |     |     |     |       |
| CLK Frequency                     | $f_{CLK}$  | $V_{DD} = +5V \pm 10\%$ |     |     | 20  | MHz   |
|                                   |            | $V_{DD} = +3V \pm 10\%$ |     |     | 10  |       |
| DIN to CLK Setup Time             | $t_{DS}$   | $V_{DD} = +5V \pm 10\%$ | 10  |     |     | ns    |
|                                   |            | $V_{DD} = +3V \pm 10\%$ | 16  |     |     |       |
| DIN to CLK Hold Time              | $t_{DH}$   | $V_{DD} = +5V \pm 10\%$ | 3   |     |     | ns    |
|                                   |            | $V_{DD} = +3V \pm 10\%$ | 3   |     |     |       |
| CLK to $\overline{LE}$ Setup Time | $t_{CS}$   | $V_{DD} = +5V \pm 10\%$ | 36  |     |     | ns    |
|                                   |            | $V_{DD} = +3V \pm 10\%$ | 65  |     |     |       |
| $\overline{LE}$ Low-Pulse Width   | $t_{WL}$   | $V_{DD} = +5V \pm 10\%$ | 14  |     |     | ns    |
|                                   |            | $V_{DD} = +3V \pm 10\%$ | 22  |     |     |       |
| CLR High-Pulse Width              | $t_{WC}$   | $V_{DD} = +5V \pm 10\%$ | 20  |     |     | ns    |
|                                   |            | $V_{DD} = +3V \pm 10\%$ | 40  |     |     |       |
| CLK Rise and Fall Times           | $t_R, t_F$ | $V_{DD} = +5V \pm 10\%$ |     |     | 50  | ns    |
|                                   |            | $V_{DD} = +3V \pm 10\%$ |     |     | 50  |       |
| CLK to DOUT Delay                 | $t_{DO}$   | $V_{DD} = +5V \pm 10\%$ | 6   |     | 42  | ns    |
|                                   |            | $V_{DD} = +3V \pm 10\%$ | 12  |     | 80  |       |

**Note 2:** All devices are 100% tested at  $T_A = +70^\circ C$ . Limits over the operating temperature range are guaranteed by design and characterization.

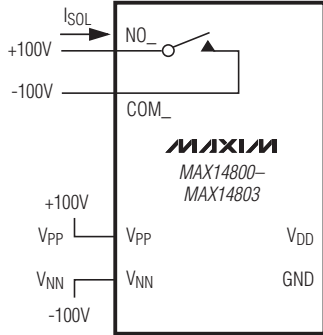
**Note 3:** The analog signal input  $V_{COM\_}$  and  $V_{NO\_}$  must satisfy  $V_{NN} \leq (V_{COM\_}, V_{NO\_}) \leq V_{PP}$ , or remain unconnected during power-up and power-down.

**Note 4:** Guaranteed by characterization; not production tested.

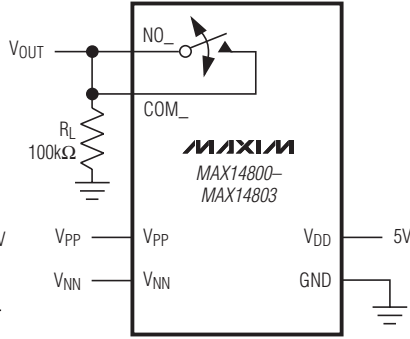
# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

## Test Circuits

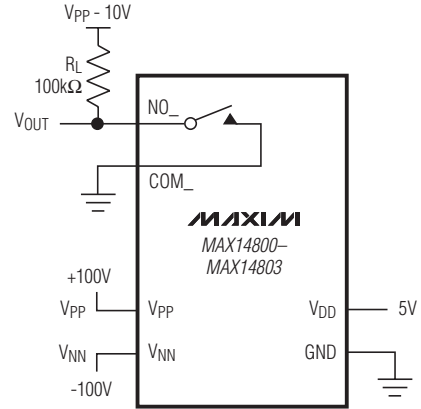
MAX14800-MAX14803



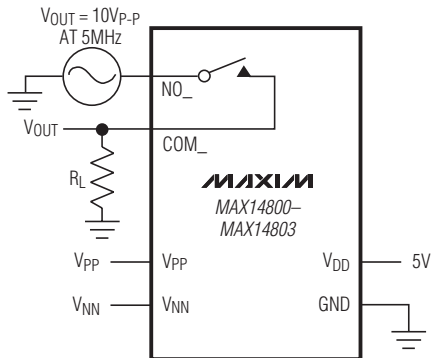
SWITCH OFF LEAKAGE



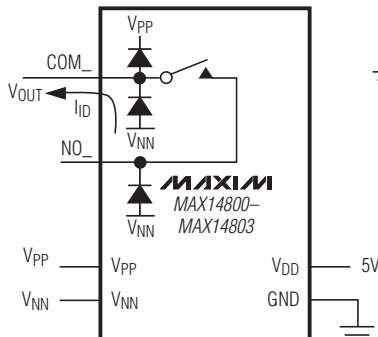
DC OFFSET ON/OFF



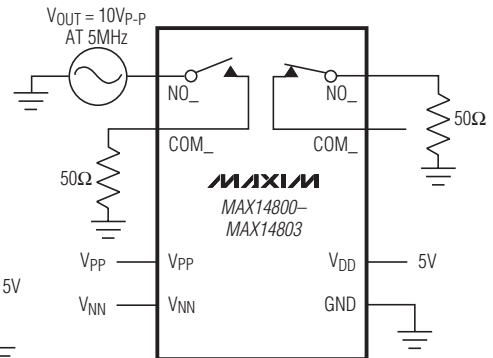
$t_{ON}/t_{OFF}$  TEST CIRCUIT



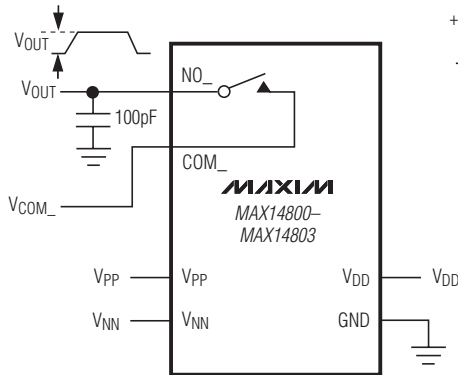
$V_{ISO} = 20 \log \frac{V_{OUT}}{V_{IN}}$   
OFF ISOLATION



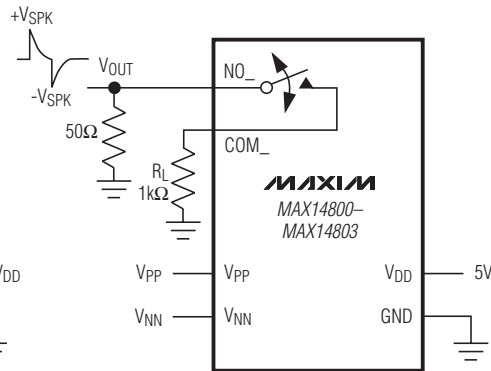
ISOLATION DIODE CURRENT



$V_{CT} = 20 \log \frac{V_{OUT}}{V_{IN}}$   
CROSSTALK



$Q = 1000\text{pF} \times V_{OUT}$   
CHARGE INJECTION

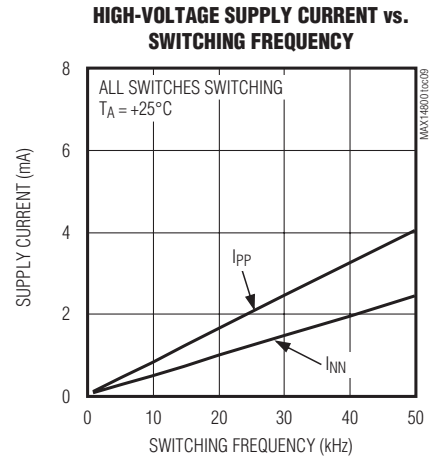
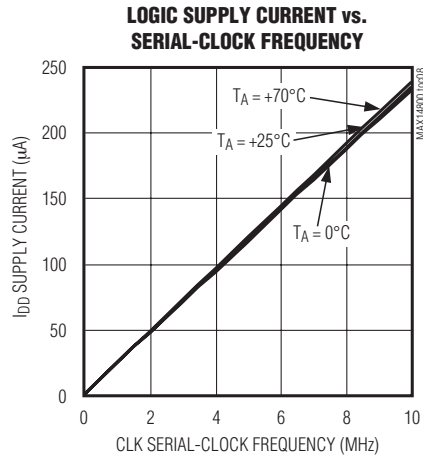
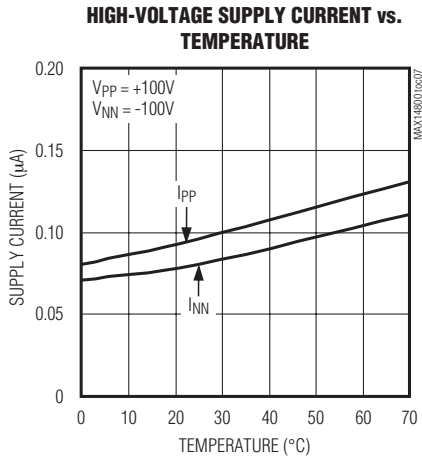
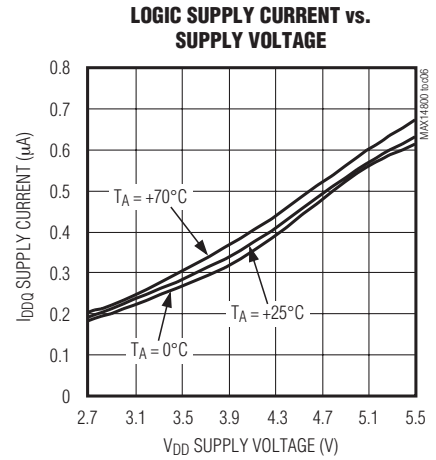
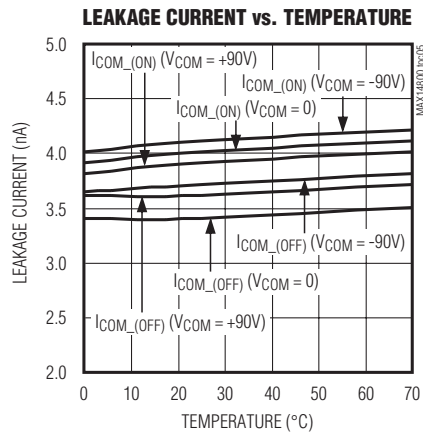
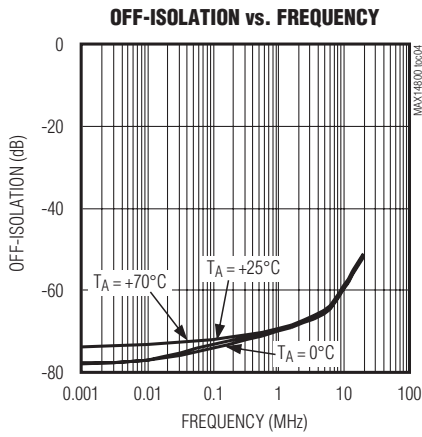
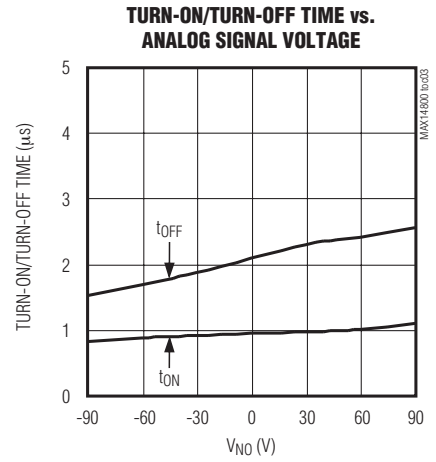
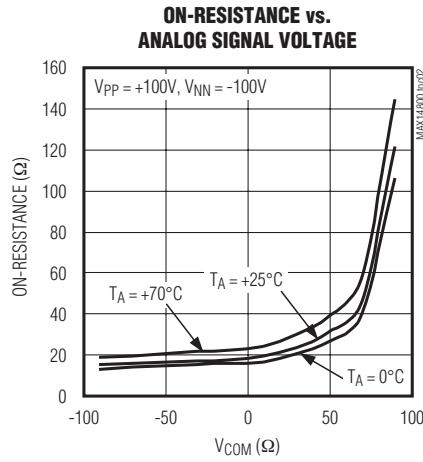
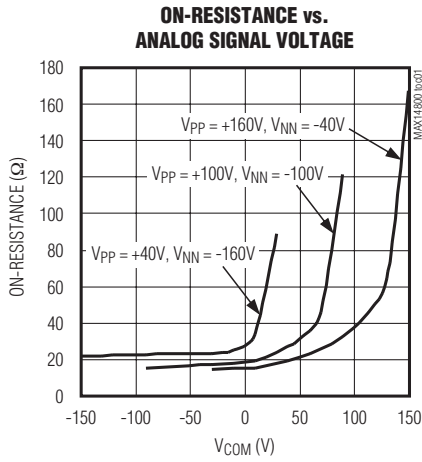


OUTPUT-VOLTAGE SPIKE

# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

## Typical Operating Characteristics

( $V_{DD} = +3V$ ,  $V_{PP} = +100V$ ,  $V_{NN} = -100V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

## Pin Description

MAX14800-MAX14803

| PIN                      | NAME                   | FUNCTION   |
|--------------------------|------------------------|--|
| 1, 2, 14, 16, 24, 35, 36 | N.C.                   | No Connection. Not internally connected.   |
| 3                        | COM4                   | Analog Switch 4—Common Terminal  |
| 4                        | NO4                    | Analog Switch 4—Normally Open Terminal   |
| 5                        | NO3                    | Analog Switch 3—Normally Open Terminal   |
| 6                        | COM3                   | Analog Switch 3—Common Terminal  |
| 7                        | NO2                    | Analog Switch 2—Normally Open Terminal   |
| 8                        | COM2                   | Analog Switch 2—Common Terminal  |
| 9                        | COM1                   | Analog Switch 1—Common Terminal  |
| 10                       | NO1                    | Analog Switch 1—Normally Open Terminal   |
| 11                       | NO0                    | Analog Switch 0—Normally Open Terminal   |
| 12                       | COM0                   | Analog Switch 0—Common Terminal  |
| 13                       | V <sub>NN</sub>        | Negative High-Voltage Supply. Bypass V <sub>NN</sub> to GND with a 0.1μF or greater ceramic capacitor. |
| 15                       | V <sub>PP</sub>        | Positive High-Voltage Supply. Bypass V <sub>PP</sub> to GND with a 0.1μF or greater ceramic capacitor. |
| 17                       | GND                    | Ground   |
| 18                       | V <sub>DD</sub>        | Digital Supply Voltage. Bypass V <sub>DD</sub> to GND with a 0.1μF or greater ceramic capacitor.       |
| 19                       | DIN                    | Serial-Data Input  |
| 20                       | CLK                    | Serial-Clock Input   |
| 21                       | $\overline{\text{LE}}$ | Active-Low, Latch-Enable Input   |
| 22                       | CLR                    | Latch Clear Input  |
| 23                       | DOUT                   | Serial-Data Output   |
| 25                       | COM15                  | Analog Switch 15—Common Terminal   |
| 26                       | NO15                   | Analog Switch 15—Normally Open Terminal  |
| 27                       | NO14                   | Analog Switch 14—Normally Open Terminal  |
| 28                       | COM14                  | Analog Switch 14—Common Terminal   |
| 29                       | COM13                  | Analog Switch 13—Common Terminal   |
| 30                       | NO13                   | Analog Switch 13—Normally Open Terminal  |
| 31                       | COM12                  | Analog Switch 12—Common Terminal   |
| 32                       | NO12                   | Analog Switch 12—Normally Open Terminal  |
| 33                       | NO11                   | Analog Switch 11—Normally Open Terminal  |
| 34                       | COM11                  | Analog Switch 11—Common Terminal   |
| 37                       | COM10                  | Analog Switch 10—Common Terminal   |

# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

## Pin Description (continued)

| PIN | NAME | FUNCTION                                |
|-----|------|---|
| 38  | NO10 | Analog Switch 10—Normally Open Terminal |
| 39  | COM9 | Analog Switch 9—Common Terminal         |
| 40  | NO9  | Analog Switch 9—Normally Open Terminal  |
| 41  | COM8 | Analog Switch 8—Common Terminal         |
| 42  | NO8  | Analog Switch 8—Normally Open Terminal  |
| 43  | NO7  | Analog Switch 7—Normally Open Terminal  |
| 44  | COM7 | Analog Switch 7—Common Terminal         |
| 45  | NO6  | Analog Switch 6—Normally Open Terminal  |
| 46  | COM6 | Analog Switch 6—Common Terminal         |
| 47  | NO5  | Analog Switch 5—Normally Open Terminal  |
| 48  | COM5 | Analog Switch 5—Common Terminal         |

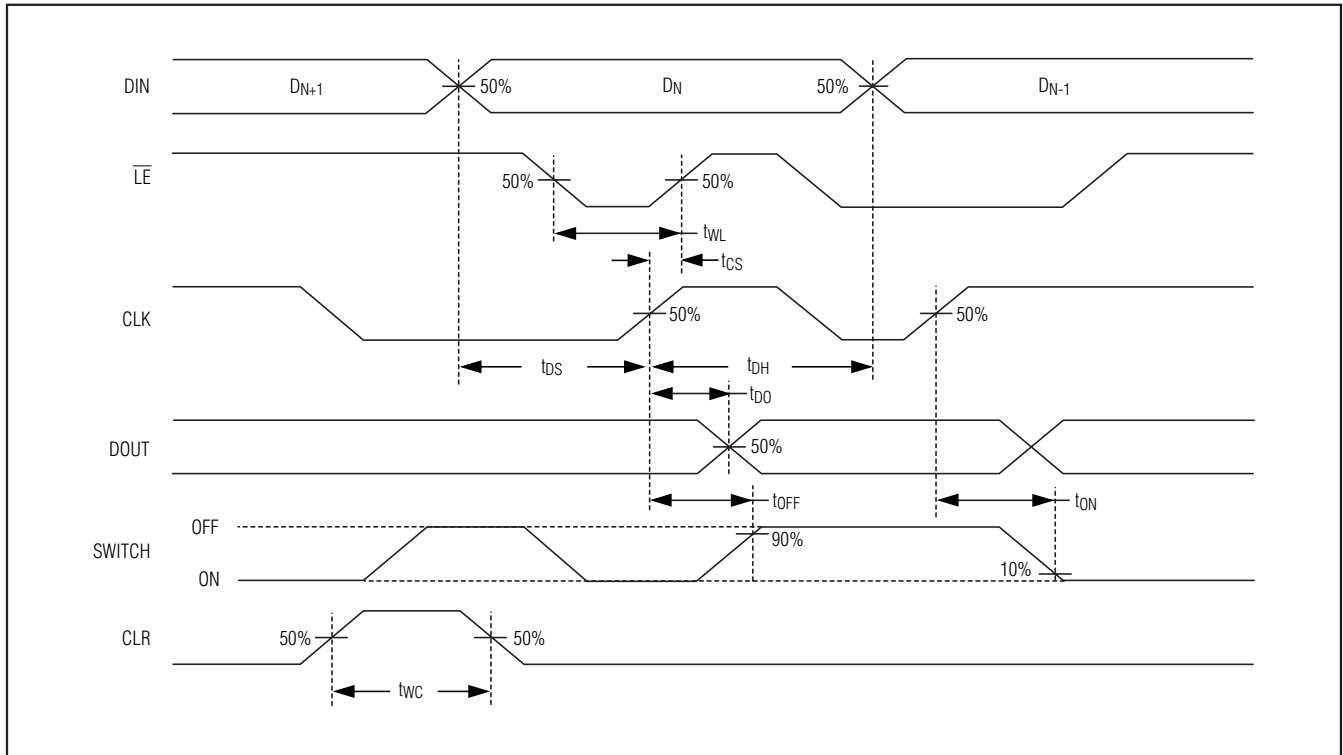


Figure 1. Serial Interface Timing



# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

MAX14800–MAX14803

## Detailed Description

The MAX14800–MAX14803 provide high-voltage switching on 16 channels for ultrasound imaging and printer applications. The devices utilize HVCMOS process technology to provide 16 high-voltage low-charge-injection SPST switches, controlled by a digital interface. Data is clocked into an internal 16-bit shift register and retained by a programmable latch with enable and clear inputs. A power-on-reset function ensures that all switches are open on power-up.

The MAX14800–MAX14803 operate with a wide range of high-voltage supplies including:  $V_{PP}/V_{NN} = +100V/-100V$ ,  $+200V/0V$ , or  $+40V/-160V$ . The digital interface operates from a separate  $+2.7V$  to  $+5.5V$   $V_{DD}$  supply. Digital inputs DIN, CLK,  $\overline{LE}$ , and CLR operate on the  $V_{DD}$  supply voltage. The MAX14801/MAX14803 provide integrated  $35k\Omega$  bleed resistors on each switch terminal to discharge capacitive loads. The MAX14802/MAX14803 provide integrated clamping diodes for overvoltage protection against positive overshoot. The MAX14802/MAX14803 feature clamping diodes (at the COM<sub>-</sub>). These clamping diodes provide overvoltage protection against positive overshoot.

## Analog Switch

The MAX14800–MAX14803 allow a peak-to-peak analog signal range from  $V_{NN}$  to the minimum of either  $V_{NN} + 200V$  or  $(V_{PP} - 10V)$ . Analog switch inputs must be unconnected, or satisfy  $V_{NN} \leq (V_{COM-}, V_{NO-}) \leq V_{PP}$  during power-up and power-down.

## High-Voltage Supplies

The MAX14800–MAX14803 allow a wide range of high-voltage supplies. The devices operate with  $V_{NN}$  from  $-160V$  to  $0$  and  $V_{PP}$  from  $+40V$  to  $V_{NN} + 250V$ . When  $V_{NN}$  is connected to GND (single-supply applications), the devices operate with  $V_{PP}$  up to  $+200V$ . The  $V_{PP}$  and  $V_{NN}$  high-voltage supplies are not required to be symmetrical, but the voltage difference ( $V_{PP} - V_{NN}$ ) must not exceed  $250V$ .

## Bleed Resistors (MAX14801/MAX14803)

The MAX14801/MAX14803 feature integrated  $35k\Omega$  bleed resistors to discharge capacitive loads such as piezoelectric transducers. Each analog switch terminal is connected to GND with a bleed resistor.

## Overvoltage Protection (MAX14802/MAX14803)

The MAX14802/MAX14803 feature clamping diodes (at the COM<sub>-</sub>). These clamping diodes provide overvoltage protection against positive overshoot.

## Serial Interface

The MAX14800–MAX14803 are controlled by a serial interface with a 16-bit serial shift register and transparent latch. Each of the sixteen data bits controls a single analog switch (see Table 1). Data on DIN is clocked with the most significant bit (MSB) first into the shift register on the rising edge of CLK. Data is clocked out of the shift register onto DOUT on the rising edge of CLK. DOUT reflects the status of DIN, delayed by 16 clock cycles (see Figures 1 and 2).

## Latch Enable ( $\overline{LE}$ )

Drive  $\overline{LE}$  logic-low to change the contents of the latch and update the state of the high-voltage switches (Figure 2). Drive  $\overline{LE}$  logic-high to freeze the contents of the latch and prevent changes to the switch states. To reduce noise due to clock feedthrough, drive  $\overline{LE}$  logic-high while data is clocked into the shift register. After the data shift register is loaded with valid data, pulse  $\overline{LE}$  logic-low to load the contents of the shift register into the latch.

## Latch Clear (CLR)

The MAX14800–MAX14803 feature a latch clear input. Drive CLR logic-high to reset the contents of the latch to zero and open all switches. CLR does not affect the contents of the data shift register. Pulse  $\overline{LE}$  logic-low to reload the contents of the shift register into the latch.

## Power-On Reset

The MAX14800–MAX14803 feature a power-on-reset circuit to ensure all switches are open at power-on. The internal 16-bit serial shift register and latch are set to zero on power-up.

# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

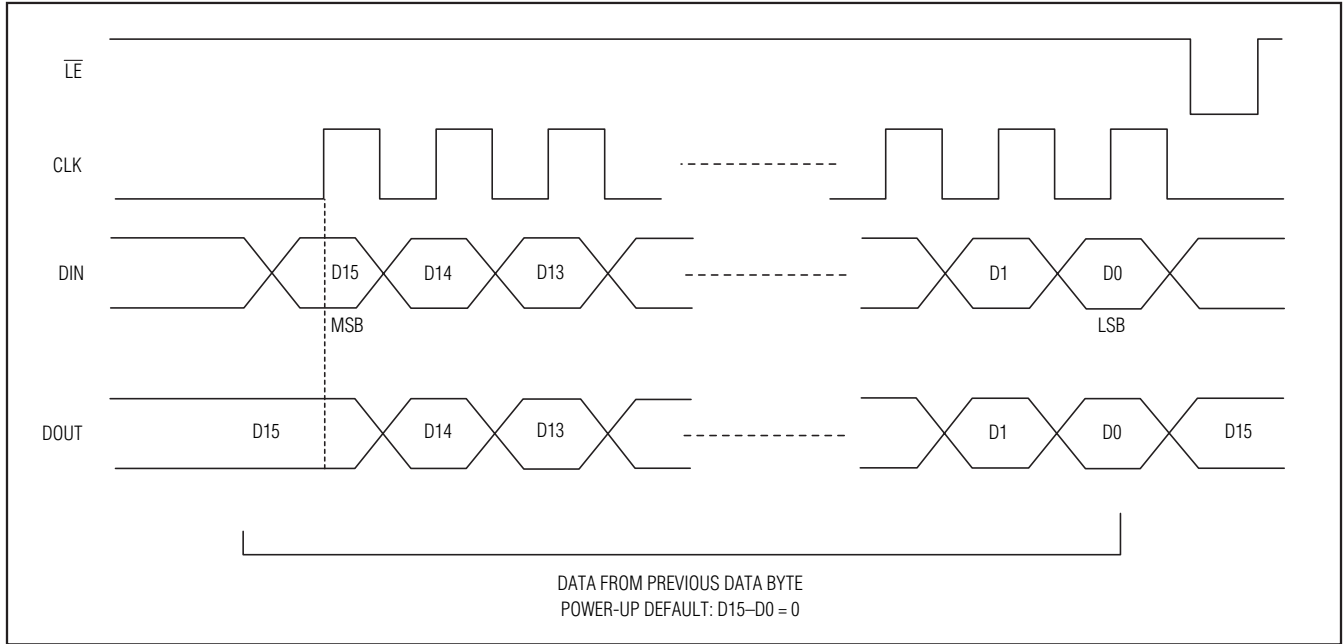


Figure 2. Latch Enable Interface Timing

Table 1. Serial Interface Programming (Notes 5–10)

| DATA BITS |    |    |    |    |    |    |    | CONTROL BITS    |     | FUNCTION            |     |     |     |     |     |     |     |     |
|-----------|----|----|----|----|----|----|----|-----------------|-----|---------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| D0 (LSB)  | D1 | D2 | D3 | D4 | D5 | D6 | D7 | $\overline{LE}$ | CLR | SW0                 | SW1 | SW2 | SW3 | SW4 | SW5 | SW6 | SW7 |     |
| L         |    |    |    |    |    |    |    | L               | L   | OFF                 |     |     |     |     |     |     |     |     |
| H         |    |    |    |    |    |    |    | L               | L   | ON                  |     |     |     |     |     |     |     |     |
|           | L  |    |    |    |    |    |    | L               | L   |                     | OFF |     |     |     |     |     |     |     |
|           | H  |    |    |    |    |    |    | L               | L   |                     | ON  |     |     |     |     |     |     |     |
|           |    | L  |    |    |    |    |    | L               | L   |                     |     | OFF |     |     |     |     |     |     |
|           |    | H  |    |    |    |    |    | L               | L   |                     |     | ON  |     |     |     |     |     |     |
|           |    |    | L  |    |    |    |    | L               | L   |                     |     |     | OFF |     |     |     |     |     |
|           |    |    | H  |    |    |    |    | L               | L   |                     |     |     | ON  |     |     |     |     |     |
|           |    |    |    | L  |    |    |    | L               | L   |                     |     |     |     | OFF |     |     |     |     |
|           |    |    |    | H  |    |    |    | L               | L   |                     |     |     |     | ON  |     |     |     |     |
|           |    |    |    |    | L  |    |    | L               | L   |                     |     |     |     |     | OFF |     |     |     |
|           |    |    |    |    | H  |    |    | L               | L   |                     |     |     |     |     | ON  |     |     |     |
|           |    |    |    |    |    | L  |    | L               | L   |                     |     |     |     |     |     |     | OFF |     |
|           |    |    |    |    |    | H  |    | L               | L   |                     |     |     |     |     |     |     | ON  |     |
| X         | X  | X  | X  | X  | X  | X  | X  | H               | L   | HOLD PREVIOUS STATE |     |     |     |     |     |     |     |     |
| X         | X  | X  | X  | X  | X  | X  | X  | X               | H   | OFF                 | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF |

# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

MAX14800-MAX14803

Table 1. Serial Interface Programming (Notes 5–10) (continued)

| DATA BITS |    |     |     |     |     |     |           | CONTROL BITS           |     | FUNCTION            |     |      |      |      |      |      |      |     |
|-----------|----|-----|-----|-----|-----|-----|-----------|------------------------|-----|---------------------|-----|------|------|------|------|------|------|-----|
| D8        | D9 | D10 | D11 | D12 | D13 | D14 | D15 (MSB) | $\overline{\text{LE}}$ | CLR | SW8                 | SW9 | SW10 | SW11 | SW12 | SW13 | SW14 | SW15 |     |
| L         |    |     |     |     |     |     |           | L                      | L   | OFF                 |     |      |      |      |      |      |      |     |
| H         |    |     |     |     |     |     |           | L                      | L   | ON                  |     |      |      |      |      |      |      |     |
|           | L  |     |     |     |     |     |           | L                      | L   |                     | OFF |      |      |      |      |      |      |     |
|           | H  |     |     |     |     |     |           | L                      | L   |                     | ON  |      |      |      |      |      |      |     |
|           |    | L   |     |     |     |     |           | L                      | L   |                     |     | OFF  |      |      |      |      |      |     |
|           |    | H   |     |     |     |     |           | L                      | L   |                     |     | ON   |      |      |      |      |      |     |
|           |    |     | L   |     |     |     |           | L                      | L   |                     |     |      | OFF  |      |      |      |      |     |
|           |    |     | H   |     |     |     |           | L                      | L   |                     |     |      | ON   |      |      |      |      |     |
|           |    |     |     | L   |     |     |           | L                      | L   |                     |     |      |      | OFF  |      |      |      |     |
|           |    |     |     | H   |     |     |           | L                      | L   |                     |     |      |      | ON   |      |      |      |     |
|           |    |     |     |     | L   |     |           | L                      | L   |                     |     |      |      |      | OFF  |      |      |     |
|           |    |     |     |     | H   |     |           | L                      | L   |                     |     |      |      |      | ON   |      |      |     |
|           |    |     |     |     |     | L   |           | L                      | L   |                     |     |      |      |      |      |      | OFF  |     |
|           |    |     |     |     |     | H   |           | L                      | L   |                     |     |      |      |      |      |      | ON   |     |
|           |    |     |     |     |     |     | L         | L                      | L   |                     |     |      |      |      |      |      | OFF  |     |
|           |    |     |     |     |     |     | H         | L                      | L   |                     |     |      |      |      |      |      | ON   |     |
| X         | X  | X   | X   | X   | X   | X   | X         | H                      | L   | HOLD PREVIOUS STATE |     |      |      |      |      |      |      |     |
| X         | X  | X   | X   | X   | X   | X   | X         | X                      | H   | OFF                 | OFF | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF |

X = Don't care.

**Note 5:** The 16 switches operate independently.

**Note 6:** Serial data is clocked in on the rising edge of CLK.

**Note 7:** The switches go to a state retaining their present condition on the rising edge of  $\overline{\text{LE}}$ . When  $\overline{\text{LE}}$  is low, the shift register data flows through the latch.

**Note 8:** DOUT is high when switch 15 is on.

**Note 9:** Shift register clocking has no effect on the switch states if  $\overline{\text{LE}}$  is high.

**Note 10:** The CLR input overrides all other inputs.

# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

## Applications Information

For medical ultrasound applications, see Figures 4, 5, and 6.

### Logic Levels

The MAX14800-MAX14803 digital interface inputs CLK, DIN,  $\overline{LE}$ , and CLR operate on the  $V_{DD}$  supply voltage.

### Daisy-Chaining Multiple Devices

Digital output DOUT is provided to allow the connection of multiple MAX14800-MAX14803 devices by daisy-chaining (Figure 3). Connect each DOUT to the DIN of the subsequent device in the chain. Connect CLK,  $\overline{LE}$ ,

and CLR inputs of all devices, and drive  $\overline{LE}$  logic-low to update all devices simultaneously. Drive CLR high to open all the switches simultaneously. Additional shift registers can be included anywhere in series with the MAX14800-MAX14803 data chain.

### Supply Sequencing and Bypassing

The MAX14800-MAX14803 do not require special sequencing of the  $V_{DD}$ ,  $V_{PP}$ , and  $V_{NN}$  supply voltages; however, analog switch inputs must be unconnected, or satisfy  $V_{NN} \leq (V_{COM\_}, V_{NO\_}) \leq V_{PP}$  during power-up and power-down. Bypass  $V_{DD}$ ,  $V_{PP}$ , and  $V_{NN}$  to GND with a 0.1 $\mu$ F ceramic capacitor as close as possible to the device.

## Application Diagrams

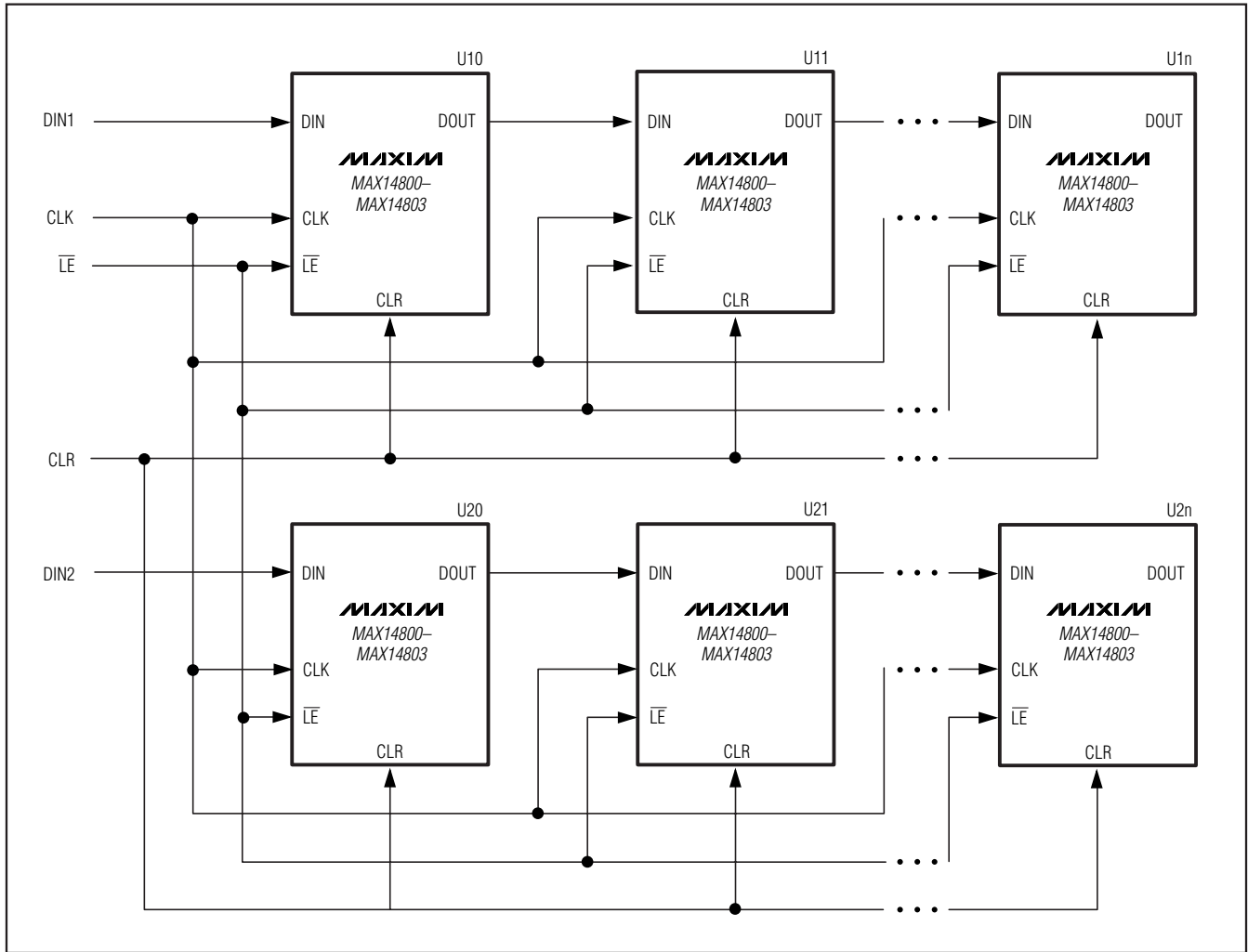


Figure 3. Interfacing Multiple Devices by Daisy-Chaining

# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

MAX14800-MAX14803

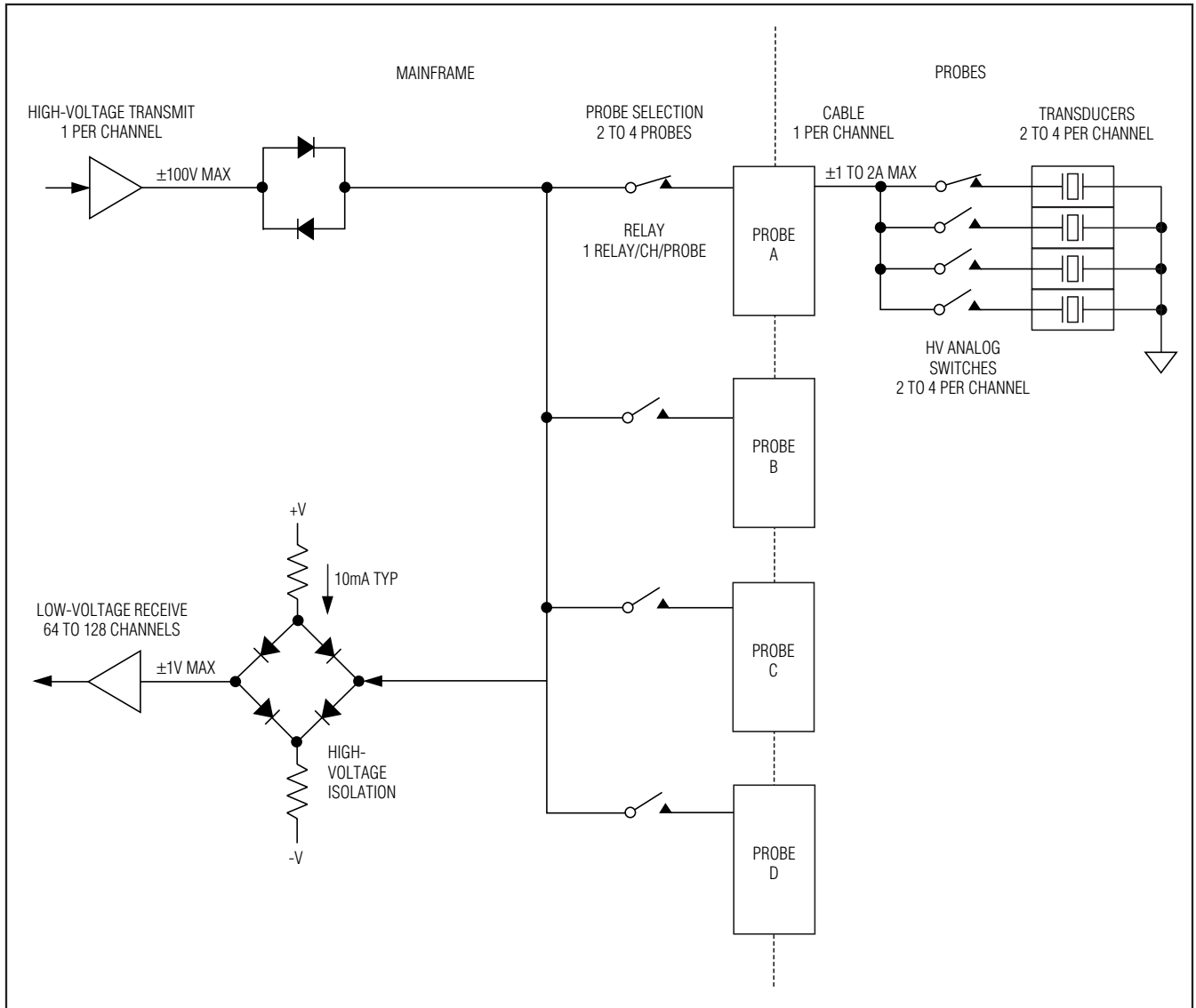


Figure 4. Medical Ultrasound Application—High-Voltage Analog Switches in Probe

# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

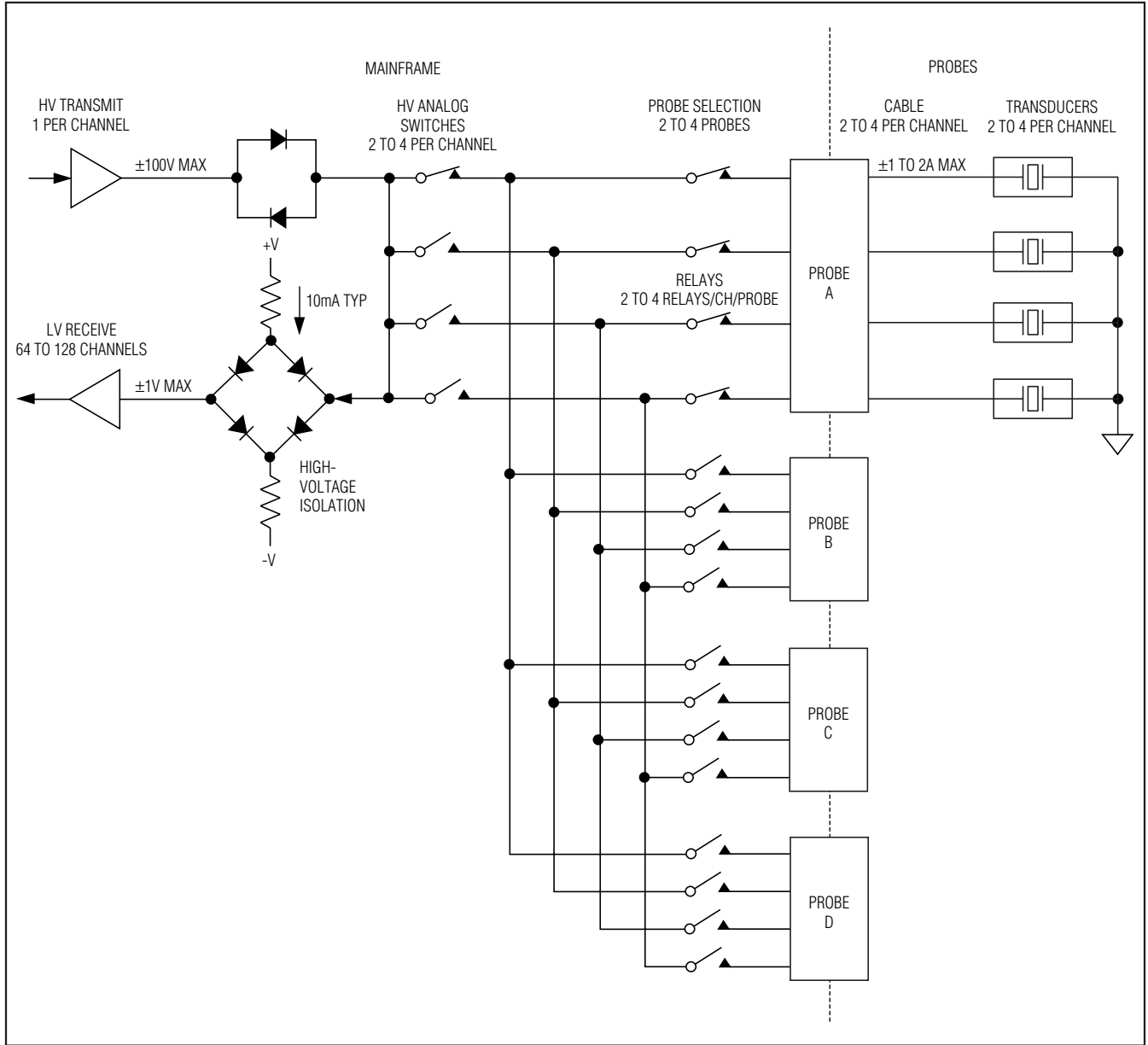


Figure 5. Medical Ultrasound Application—High-Voltage Analog Switches in Mainframe

# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

MAX14800-MAX14803

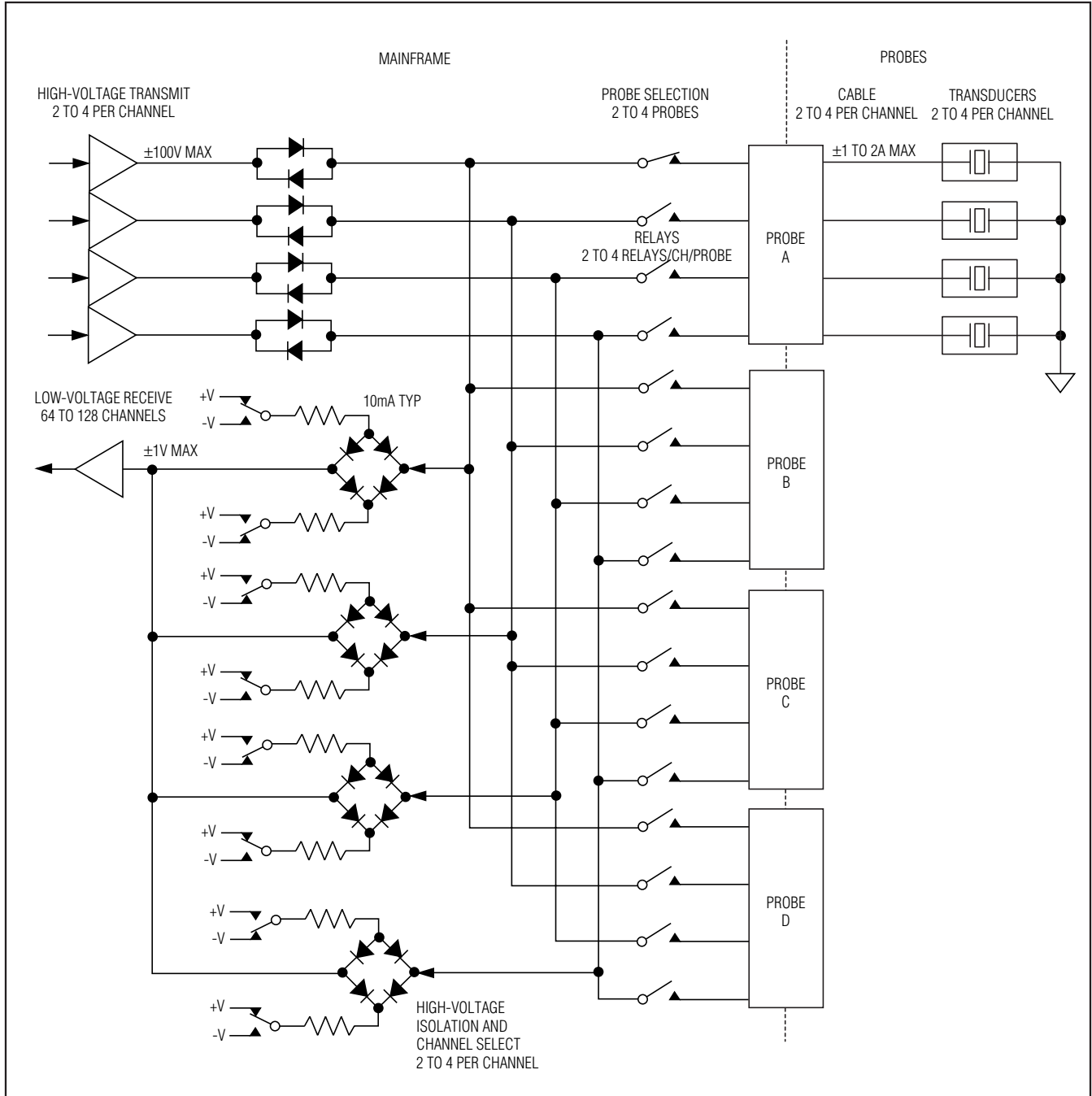
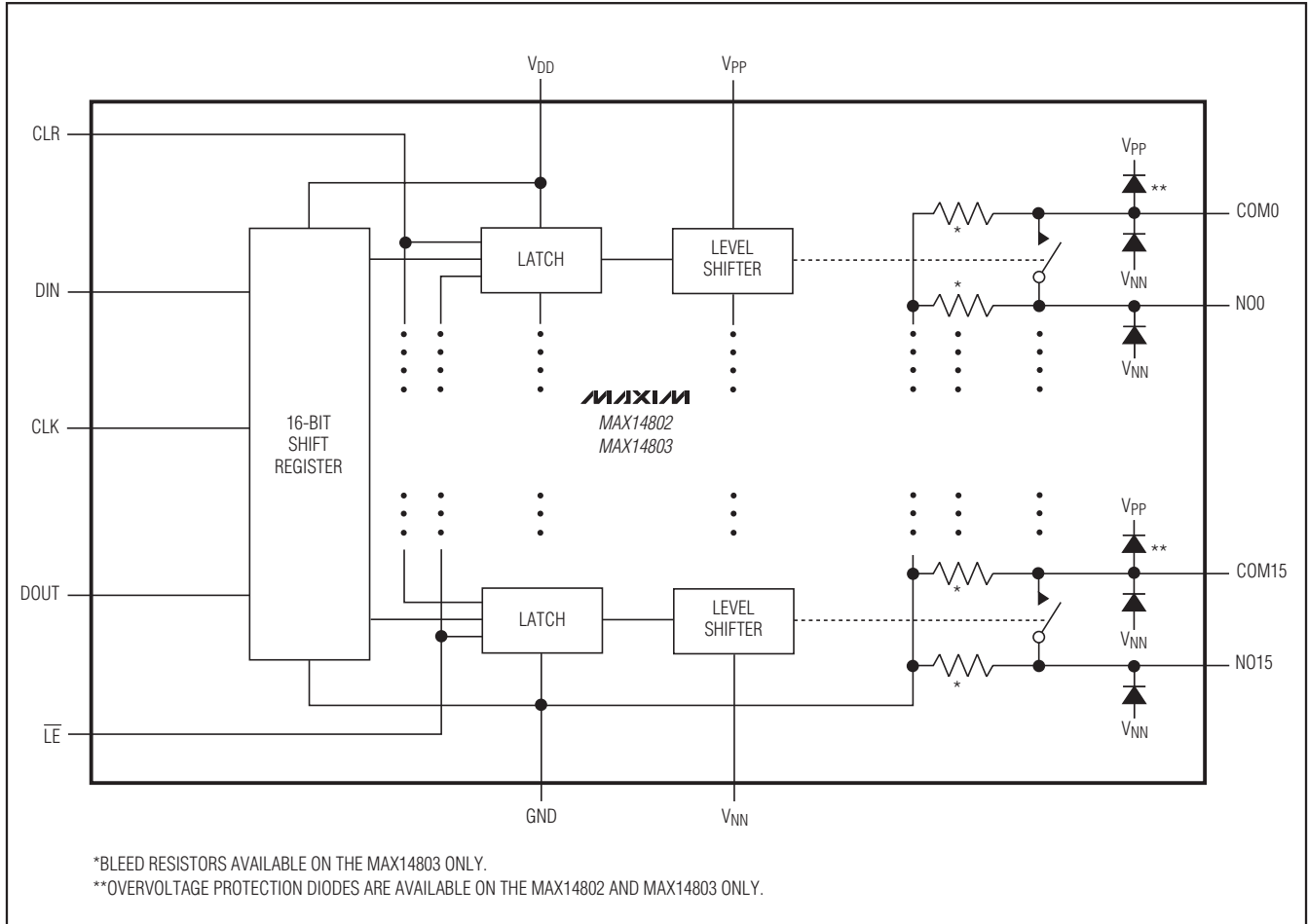


Figure 6. Medical Ultrasound Application—Multiple Transmit and Isolation per Receiver Channel

# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

## Functional Diagram

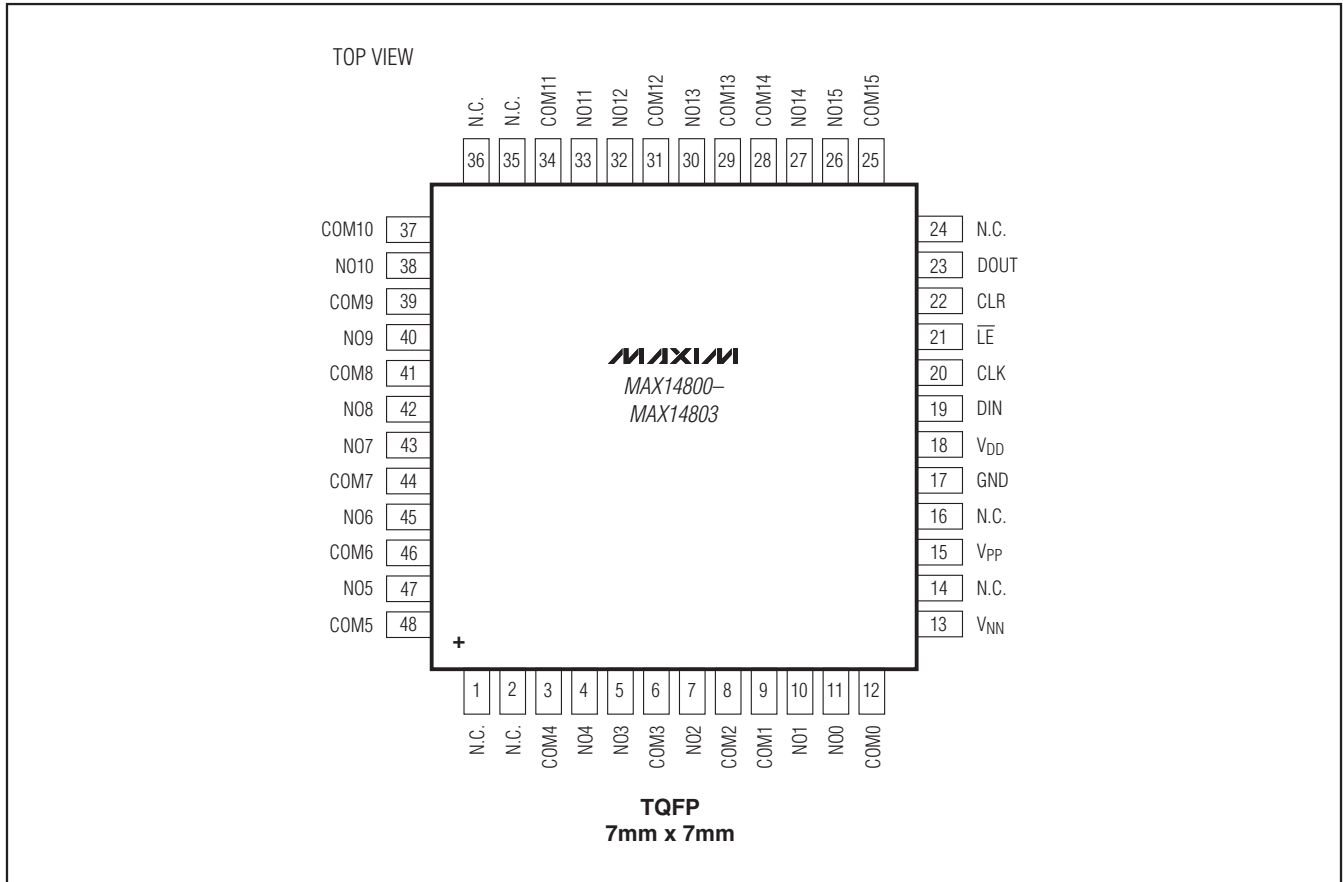




# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

## Pin Configuration

**MAX14800-MAX14803**



### Chip Information

PROCESS: BiCMOS

### Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO.            |
|--------------|--------------|-------------------------|
| 48 TQFP      | C48-6        | <a href="#">21-0054</a> |

# Low-Charge Injection, 16-Channel, High-Voltage Analog Switches

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION  | PAGES CHANGED |
|-----------------|---------------|--|---------------|
| 0               | 4/09          | Initial release.   | —             |
| 1               | 9/09          | Corrected two specifications in the <i>Absolute Maximum Ratings</i> section. Changed the minimum of the peak-to-peak analog signal range to “either $V_{NN} + 200V$ or $(V_{PP} - 10V)$ .” | 2, 9          |

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