# **Power MOSFET**

# 20 V, 3.2 A, Single N-Channel, SOT-23

### **Features**

- Leading Planar Technology for Low Gate Charge / Fast Switching
- 2.5 V Rated for Low Voltage Gate Drive
- SOT-23 Surface Mount for Small Footprint
- Pb-Free Package is Available

## **Applications**

- Load/Power Switch for Portables
- Load/Power Switch for Computing
- DC-DC Conversion

## MAXIMUM RATINGS (T<sub>J</sub>= 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage		$V_{DSS}$	20	V	
Gate-to-Source Voltage			$V_{GS}$	±12	V
Continuous Drain	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	3.2	Α
Current (Note 1)		T <sub>A</sub> = 85°C		2.4	Α
Steady State Power Dissipation (Note 1)	Steady State		P <sub>D</sub>	1.25	W
Pulsed Drain Current	t <sub>p</sub> = 10 μs		I <sub>DM</sub>	10.0	Α
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C
Continuous Source Current (Body Diode)			IS	1.6	Α
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	100	°C/W
Junction-to-Ambient (Note 2)	$R_{\theta JA}$	300	

- 1. Surface—mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
- 2. Surface-mounted on FR4 board using the minimum recommended pad size.

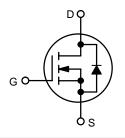


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V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX (Note 1)
20 V	70 mΩ @ 4.5 V	3.6 A
	85 mΩ @ 2.5 V	3.1 A

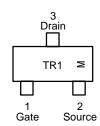
#### N-Channel





SOT-23 CASE 318 STYLE 21





TR1 = Specific Device Code M = Date Code

## **ORDERING INFORMATION**

Device	Package	Shipping†
NTR4501NT1	SOT-23	3000 / Tape & Reel
NTR4501NT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
NTR4501NT3	SOT-23	10000 / Tape & Reel
NTR4501NT3G	SOT-23 (Pb-Free)	10000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## **Electrical Characteristics** ( $T_J = 25$ °C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Тур	Max	Units
OFF CHARACTERISTICS			-			
Drain-to-Source Breakdown Voltage (Note 3)	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu$	ıA 20	24.5		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			22		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$ $T_J = 2$	5°C		1.5	μΑ
		V <sub>DS</sub> = 16 V T <sub>J</sub> = 89	5°C		10	μΑ
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12$	2 V		±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage (Note 3)	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_{D} = 250 \mu$	uA 0.65		1.2	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			-2.3		mV/°C
Drain-to-Source On Resistance		$V_{GS} = 4.5 \text{ V}, I_D = 3.6$	A	70	80	mΩ
	R <sub>DS(on)</sub>	$V_{GS} = 2.5 \text{ V}, I_D = 3.1$	A	85	105	
Forward Transconductance	9FS	$V_{DS} = 5.0 \text{ V}, I_D = 3.6$	Α	9		S
CHARGES AND CAPACITANCES			•	•	-	•
Input Capacitance	C <sub>iss</sub>			200		pF
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz}$ $V_{DS} = 10 \text{ V}$	z,	80		
Reverse Transfer Capacitance	C <sub>rss</sub>	103 .01		50		
Total Gate Charge	Q <sub>G(TOT)</sub>			2.4	6.0	
Gate-to-Source Gate Charge	$Q_{GS}$	$V_{GS} = 4.5 \text{ V}, V_{DS} = 10$ $I_{D} = 3.6 \text{ A}$	V,	0.5		nC
Gate-to-Drain Charge	$Q_{GD}$	.g <b>0.0</b> 71		0.6		
SWITCHING CHARACTERISTICS (Note 4)			•	•	-	•
Turn-On Delay Time	t <sub>d(on)</sub>			6.5		
Rise Time	t <sub>r</sub>	$V_{GS} = 4.5 \text{ V}, V_{DS} = 10$	V.	12		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D = 3.6 \text{ A}, R_G = 6.0 \text{ S}$	Ω΄	12		ns
Fall Time	t <sub>f</sub>			3		7 !
SOURCE-DRAIN DIODE CHARACTERISTICS	3		•	-	-	-
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0 \text{ V}, I_{SD} = 1.6 \text{ A}$	A	0.8	1.2	V
Reverse Recovery Time	t <sub>RR</sub>			7.1		
Charge Time	t <sub>a</sub>	$V_{GS} = 0 \text{ V},$		5		ns
Discharge Time	t <sub>b</sub>	$d_{1S}/d_t = 100 \text{ A/}\mu\text{s},$ $I_S = 1.6 \text{ A}$		1.9		
Reverse Recovery Charge	Q <sub>RR</sub>			3.0		nC

Pulse Test: Pulse width ≤ 300 μs, duty cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

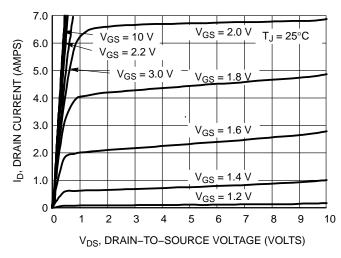


Figure 1. On-Region Characteristics

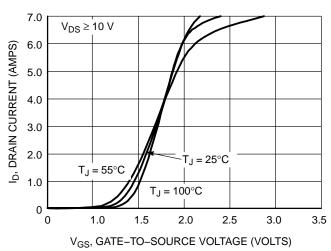


Figure 2. Transfer Characteristics

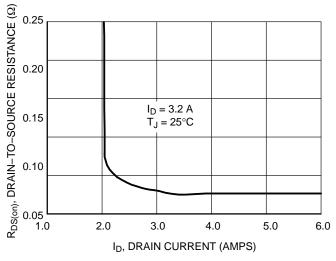


Figure 3. On–Resistance versus Gate–to–Source Voltage

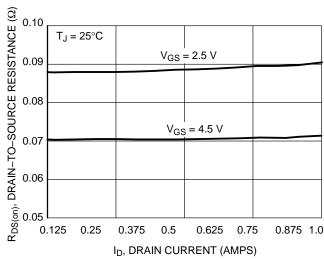


Figure 4. On–Resistance versus Drain Current and Gate Voltage

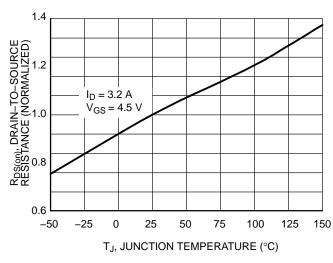


Figure 5. On–Resistance Variation with Temperature

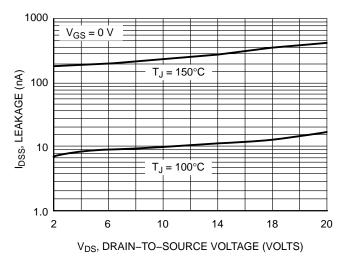


Figure 6. Drain-to-Source Leakage
Current versus Voltage

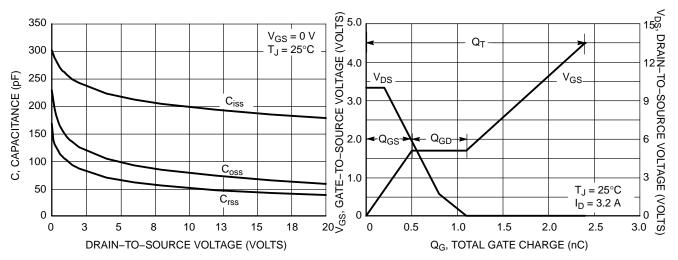


Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

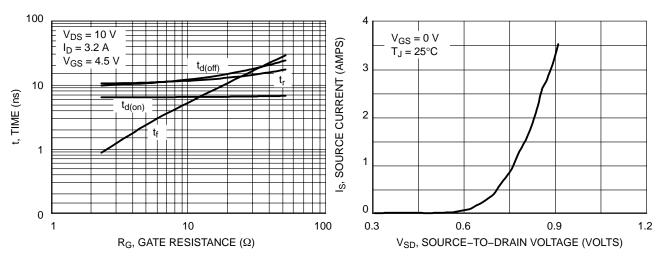
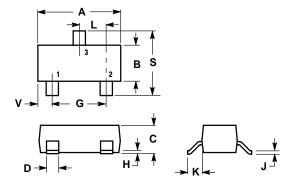


Figure 9. Resistive Switching Time Variation versus Gate Resistance

Figure 10. Diode Forward Voltage versus Current

## **PACKAGE DIMENSIONS**

SOT-23 (TO-236)CASE 318-08 **ISSUE AK** 



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF PASE MATERIAL
- BASE MATERIAL.
  4. 318–01 THRU –07 AND –09 OBSOLETE, NEW STANDARD 318–08.

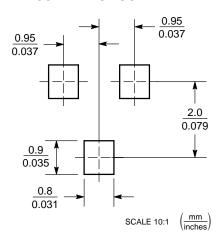
	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.1102	0.1197	2.80	3.04	
В	0.0472	0.0551	1.20	1.40	
С	0.0350	0.0440	0.89	1.11	
D	0.0150	0.0200	0.37	0.50	
G	0.0701	0.0807	1.78	2.04	
Н	0.0005	0.0040	0.013	0.100	
J	0.0034	0.0070	0.085	0.177	
K	0.0140	0.0285	0.35	0.69	
L	0.0350	0.0401	0.89	1.02	
S	0.0830	0.1039	2.10	2.64	
V	0.0177	0.0236	0.45	0.60	

STYLE 21:

PIN 1. GATE 2. SOURCE

- 3. DRAIN

## **SOLDERING FOOTPRINT\***



<sup>\*</sup>For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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