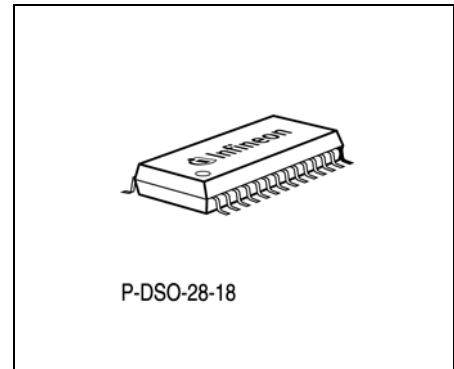


## Overview

### Features

- Driver for up to 3 motors
- Delivers up to 0.8 A continuous
- Optimized for DC motor management applications
- Very low current consumption in stand-by (Inhibit) mode
- Low saturation voltage; typ.1.2 V total @ 25 °C; 0.4 A
- Output protected against short circuit
- Error flag diagnosis
- Overvoltage lockout and diagnosis
- Undervoltage lockout
- CMOS/TTL compatible inputs with hysteresis
- No crossover current
- Internal clamp diodes
- Overtemperature protection with hysteresis and diagnosis
- Enhanced power P-DSO-Package



Type	Ordering Code	Package
TLE 4208 G	Q67007-A9335	P-DSO-28-18

### Description

The TLE 4208 is a fully protected **Quad-Half-Bridge-Driver** designed specially for automotive and industrial motion control applications.

The part is built using the Siemens bipolar high voltage power technology DOPL.

In a cascade configuration up to three actuators (DC motors) can be connected between the four half-bridges. These four half-bridges are configured as 2 dual-half-bridges, which are supplied and controlled separately. Operation modes forward (cw), reverse (ccw), brake and high impedance are invoked from a standard interface.

The standard enhanced power P-DSO-28 package meets the application requirements and saves PCB-board space and costs.

Furthermore the built-in features like diagnosis, over- and undervoltage-lockout, short-circuit protection, over-temperature protection and the very low quiescent current in stand-by mode will open a wide range of automotive and industrial applications.

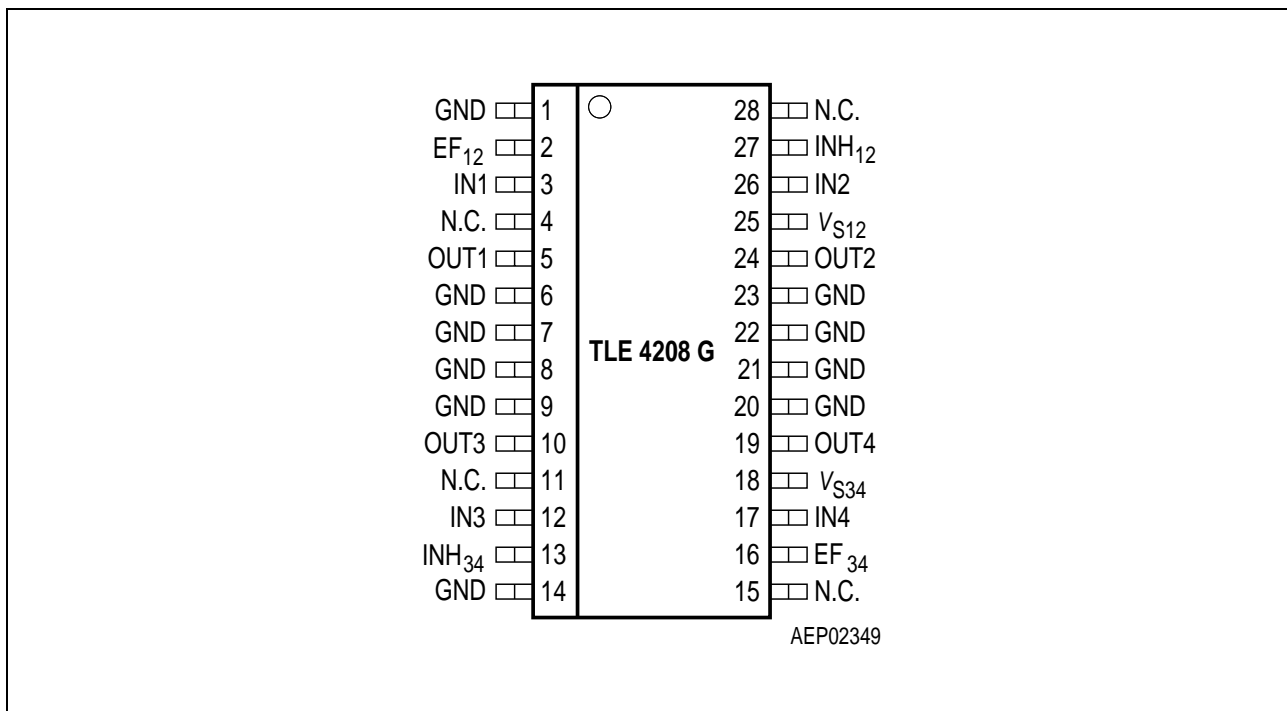


Figure 1 Pin Configuration (top view)

**Pin Definitions and Functions**

Pin No.	Symbol	Function
1, 6, 7, 8, 9, 14, 20, 21, 22, 23	GND	<b>Ground;</b> negative reference potential for blocking capacitor
2	EF <sub>12</sub>	<b>Error Flag output of half-bridges 1 and 2;</b> open collector; low = error
3	IN1	<b>Input channel of half-bridge 1;</b> controls OUT1
4, 11, 15, 28	N.C.	<b>Not connected</b>
5	OUT1	<b>Power output of half-bridge 1;</b> full short circuit protected; with integrated clamp diodes
10	OUT3	<b>Power output of half-bridge 3;</b> full short-circuit protected; with integrated clamp diodes
12	IN3	<b>Input channel of half-bridge 3;</b> controls OUT3
13	INH <sub>34</sub>	<b>Inhibit input of half-bridges 3 and 4;</b> low = half-bridges 3 and 4 in stand-by
16	EF <sub>34</sub>	<b>Error Flag output of half-bridges 3 and 4;</b> open collector; low = error
17	IN4	<b>Input channel of half-bridge 4;</b> controls OUT4
18	V <sub>S34</sub>	<b>Power supply voltage of half-bridges 3 and 4;</b> positive reference potential for blocking capacitor
19	OUT4	<b>Power output of half-bridge 4;</b> full short circuit protected; with integrated clamp diodes
24	OUT2	<b>Power-output of half-bridge 2;</b> full short circuit protected; with integrated clamp diodes
25	V <sub>S12</sub>	<b>Power supply voltage of half-bridges 1 and 2;</b> positive reference potential for blocking capacitor
26	IN2	<b>Input channel of half-bridge 2;</b> controls OUT2
27	INH <sub>12</sub>	<b>Inhibit input of half-bridges 1 and 2;</b> low = half-bridges 1 and 2 in stand-by

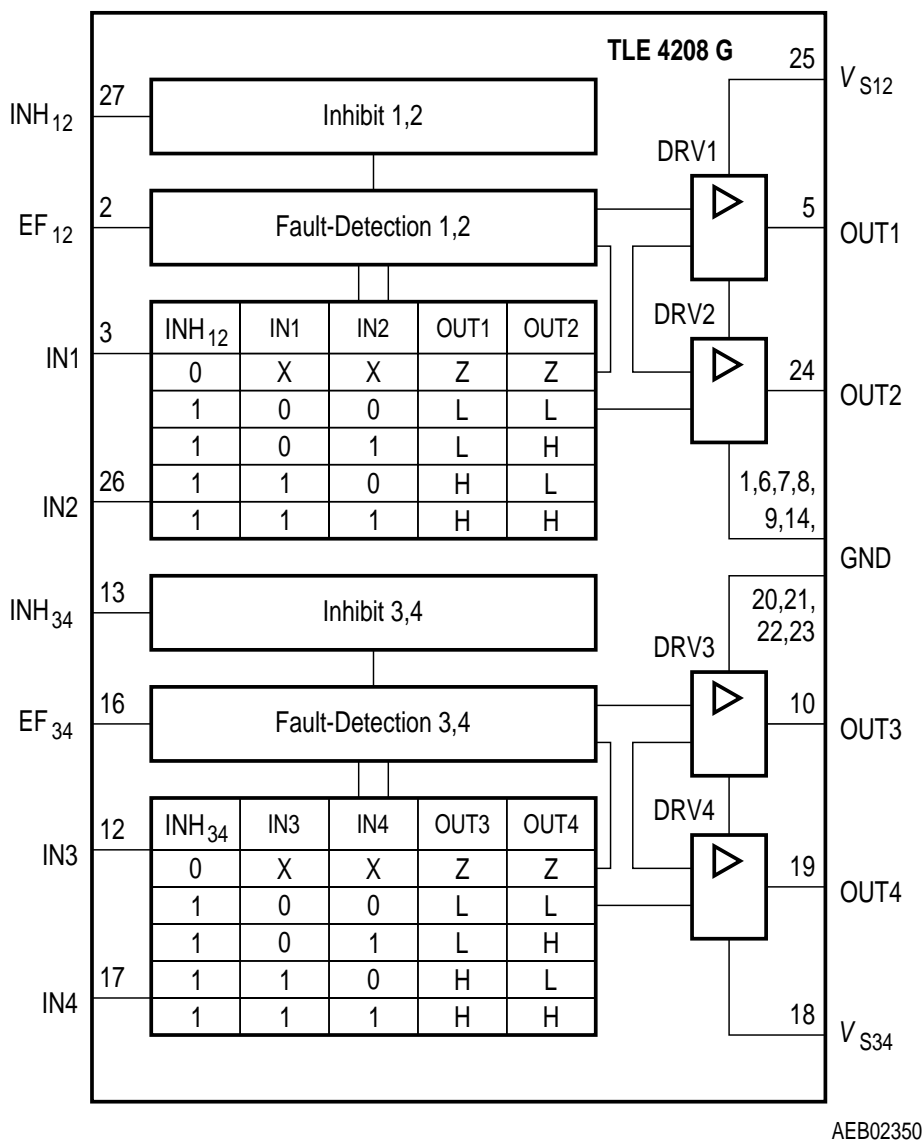


Figure 2 Block Diagram

## Input Logic

### Functional Truth Table of Halfbridge 1 and 2

INH <sub>12</sub>	IN1	IN2	OUT1	OUT2	Mode
0	X	X	Z	Z	Stand-By
1	0	0	L	L	Brake LL
1	0	1	L	H	CW
1	1	0	H	L	CCW
1	1	1	H	H	Brake HH

*Note: Half-Bridge 1 and 2 connected to a full-bridge*

### Functional Truth Table of Half-Bridge 3 and 4

INH <sub>34</sub>	IN3	IN4	OUT3	OUT4	Mode
0	X	X	Z	Z	Stand-By
1	0	0	L	L	Brake LL
1	0	1	L	H	CW
1	1	0	H	L	CCW
1	1	1	H	H	Brake HH

IN: 0 = Logic LOW  
 1 = Logic HIGH  
 X = don't care

OUT: Z = Output in tristate condition  
 L = Output in sink condition  
 H = Output in source condition

*Note: Half-Bridge 3 and 4 connected to a full-bridge*

## Diagnosis

EF <sub>12</sub>	EF <sub>34</sub>	Error
1	1	no error
0	1	over temperature of half-bridge 1 and 2 or over voltage of half-bridge 1 and 2
0	1	over temperature of half-bridge 3 and 4 or over voltage of half-bridge 3 and 4
1	0	over temperature of all half-bridges or over voltage of all half-bridges
1	0	over temperature of all half-bridges or over voltage of all half-bridges
0	0	over temperature of all half-bridges or over voltage of all half-bridges
0	0	over temperature of all half-bridges or over voltage of all half-bridges

**Electrical Characteristics**
**Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

**Voltages**

Supply voltage	$V_{S12}, V_{S34}$	- 0.3	45	V	-
Supply voltage	$V_{S12}, V_{S34}$	- 1	-	V	$t < 0.5 \text{ s}; I_{S12}, I_{S34} > - 2 \text{ A}$
Logic input voltages (IN1; IN2; INH <sub>12</sub> ; IN3; IN4; INH <sub>34</sub> )	$V_I$	- 5	20	V	$0 \text{ V} < V_{S12}, V_{S34} < 45 \text{ V}$
Logic output voltage (EF <sub>12</sub> ; EF <sub>34</sub> )	$V_{EF12}, V_{EF34}$	- 0.3	20	V	$0 \text{ V} < V_{S12}, V_{S34} < 45 \text{ V}$

**Currents**

Output current (cont.)	$I_{OUT1-4}$	-	-	A	internally limited
Output current (peak)	$I_{OUT1-4}$	-	-	A	internally limited
Output current (diode)	$I_{OUT1-4}$	-1	1	A	-
Output current (EF)	$I_{EF12-34}$	-2	5	mA	-

**Temperatures**

Junction temperature	$T_j$	- 40	150	°C	-
Storage temperature	$T_{stg}$	- 50	150	°C	-

**Thermal Resistances**

Junction pin	$R_{thj-pin}$	-	25	K/W	measured to pin 7
Junction ambient	$R_{thjA}$	-	65	K/W	-

*Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.*

**Operating Range**

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	$V_{S12}, V_{S34}$	$V_{UV\ OFF}$	18	V	After $V_{S12}, V_{S34}$ rising above $V_{UV\ ON}$
Supply voltage increasing	$V_{S12}, V_{S34}$	- 0.3	$V_{UV\ ON}$	V	Outputs in tristate
Supply voltage decreasing	$V_{S12}, V_{S34}$	- 0.3	$V_{UV\ OFF}$	V	Outputs in tristate
Logic input voltages (IN1; IN2; INH <sub>12</sub> ; IN3; IN4; INH <sub>34</sub> )	$V_I$	- 2	18	V	-
Junction temperature	$T_j$	- 40	150	°C	-

*Note: In the operating range the functions given in the circuit description are fulfilled.*

**Electrical Characteristics**

8 V <  $V_{S12} = V_{S34} < 18$  V;  $INH_{12} = INH_{34} = \text{HIGH}$ ;  $I_{OUT1-4} = 0$  A;  $-40$  °C <  $T_j < 150$  °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Current Consumption**

$INH_{12} = INH_{34} = \text{LOW}$

Quiescent current	$I_S$	–	–	100	μA	$I_S = I_{S12} + I_{S34}$
Quiescent current	$I_S$	–	20	40	μA	$I_S = I_{S12} + I_{S34}$ ; $V_{S12} = V_{S34} = 13.2$ V; $T_j = 25$ °C

$INH_{12} = \text{HIGH}$  and  $INH_{34} = \text{LOW}$  or  $INH_{12} = \text{LOW}$  and  $INH_{34} = \text{HIGH}$

Supply current	$I_{S12}, I_{S34}$	–	10	20	mA	–
Supply current	$I_{S12}, I_{S34}$	–	–	30	mA	$I_{OUT1/3} = 0.4$ A $I_{OUT2/4} = -0.4$ A
Supply current	$I_{S12}, I_{S34}$	–	–	50	mA	$I_{OUT1/3} = 0.8$ A $I_{OUT2/4} = -0.8$ A

**Over- and Under Voltage Lockout**

UV Switch ON voltage	$V_{UV\ ON}$	–	6.5	7.5	V	$V_{S12}, V_{S34}$ increasing
UV Switch OFF voltage	$V_{UV\ OFF}$	5	6	–	V	$V_{S12}, V_{S34}$ decreasing
UV ON/OFF hysteresis	$V_{UV\ HY}$	–	0.5	–	V	$V_{UV\ ON} - V_{UV\ OFF}$
OV Switch OFF voltage	$V_{OV\ OFF}$	–	20	24	V	$V_{S12}, V_{S34}$ increasing
OV Switch ON voltage	$V_{OV\ ON}$	18	19.5	–	V	$V_{S12}, V_{S34}$ decreasing
OV ON/OFF hysteresis	$V_{OV\ HY}$	–	0.5	–	V	$V_{OV\ OFF} - V_{OV\ ON}$



**Electrical Characteristics (cont'd)**

8 V <  $V_{S12} = V_{S34} < 18$  V;  $INH_{12} = INH_{34} = HIGH$ ;  $I_{OUT1-4} = 0$  A;  $-40$  °C <  $T_j < 150$  °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Outputs OUT1; OUT2; OUT 3; OUT 4**
**Saturation Voltages**

Source (upper) $I_{OUT12}, I_{OUT34} = -0.2$ A	$V_{SAT U}$	–	0.85	1.15	V	$T_j = 25$ °C
Source (upper) $I_{OUT12}, I_{OUT34} = -0.4$ A	$V_{SAT U}$	–	0.90	1.20	V	$T_j = 25$ °C
Sink (upper) $I_{OUT12}, I_{OUT34} = -0.8$ A	$V_{SAT U}$	–	1.10	1.50	V	$T_j = 25$ °C
Sink (lower) $I_{OUT12}, I_{OUT34} = 0.2$ A	$V_{SAT L}$	–	0.15	0.23	V	$T_j = 25$ °C
Sink (lower) $I_{OUT12}, I_{OUT34} = 0.4$ A	$V_{SAT L}$	–	0.25	0.40	V	$T_j = 25$ °C
Sink (lower) $I_{OUT12}, I_{OUT34} = 0.8$ A	$V_{SAT L}$	–	0.45	0.75	V	$T_j = 25$ °C

Total Drop $I_{OUT12}, I_{OUT34} = 0.2$ A	$V_{SAT}$	–	1	1.4	V	$V_{SAT} = V_{SAT U} + V_{SAT L}$
Total Drop $I_{OUT12}, I_{OUT34} = 0.4$ A	$V_{SAT}$	–	1.2	1.7	V	$V_{SAT} = V_{SAT U} + V_{SAT L}$
Total Drop $I_{OUT12}, I_{OUT34} = 0.8$ A	$V_{SAT}$	–	1.6	2.5	V	$V_{SAT} = V_{SAT U} + V_{SAT L}$

**Clamp Diodes**

Forward voltage; upper	$V_{FU}$	–	1	1.5	V	$I_F = 0.4$ A
Upper leakage current	$I_{LKU}$	–	–	5	mA	$I_F = 0.4$ A <sup>1)</sup>
Forward voltage; lower	$V_{FL}$	–	0.9	1.4	V	$I_F = 0.4$ A

Notes see page 11.

**Electrical Characteristics (cont'd)**

$8\text{ V} < V_{S12} = V_{S34} < 18\text{ V}$ ;  $\text{INH}_{12} = \text{INH}_{34} = \text{HIGH}$ ;  $I_{\text{OUT}1-4} = 0\text{ A}$ ;  $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$ ;  
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Input Interface**
**Logic Inputs IN1; IN2; IN3; IN4**

H-input voltage	$V_{\text{IH}}$	–	2.0	3.0	V	–
L-input voltage	$V_{\text{IL}}$	1.0	1.5	–	V	–
Hysteresis of input voltage	$V_{\text{IHY}}$	–	0.5	–	V	–
H-input current	$I_{\text{IH}}$	– 2	–	10	$\mu\text{A}$	$V_{\text{I}} = 5\text{ V}$
L-input current	$I_{\text{IL}}$	– 100	– 20	– 5	$\mu\text{A}$	$V_{\text{I}} = 0\text{ V}$

**Logic Inputs INH<sub>12</sub>; INH<sub>34</sub>**

H-input voltage	$V_{\text{IH}}$	–	2.7	3.5	V	–
L-input voltage	$V_{\text{IL}}$	1.0	2.0	–	V	–
Hysteresis of input voltage	$V_{\text{IHY}}$	–	0.7	–	V	–
H-input current	$I_{\text{IH}}$	–	100	250	$\mu\text{A}$	$V_{\text{INH}} = 5\text{ V}$
L-input current	$I_{\text{IL}}$	– 10	–	10	$\mu\text{A}$	$V_{\text{INH}} = 0\text{ V}$

**Error-Flags EF<sub>12</sub>; EF<sub>34</sub>**

L-output voltage level	$V_{\text{EFL}}$	–	0.2	0.4	V	$I_{\text{EF}} = 2\text{ mA}$
Leakage current	$I_{\text{EFLK}}$	–	–	10	$\mu\text{A}$	$0\text{ V} < V_{\text{EF}} < 7\text{ V}$

**Electrical Characteristics (cont'd)**

$8\text{ V} < V_{S12} = V_{S34} < 18\text{ V}$ ;  $\text{INH}_{12} = \text{INH}_{34} = \text{HIGH}$ ;  $I_{\text{OUT}1-4} = 0\text{ A}$ ;  $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$ ;  
 unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Thermal Shutdown**

Thermal shutdown junction temperature	$T_{\text{jSD}}$	150	175	200	$^{\circ}\text{C}$	–
Thermal switch-on junction temperature	$T_{\text{jSO}}$	120	–	170	$^{\circ}\text{C}$	–
Temperature hysteresis	$\Delta T$	–	30	–	K	–

1) Guaranteed by design.

*Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25^{\circ}\text{C}$  and the given supply voltage.*

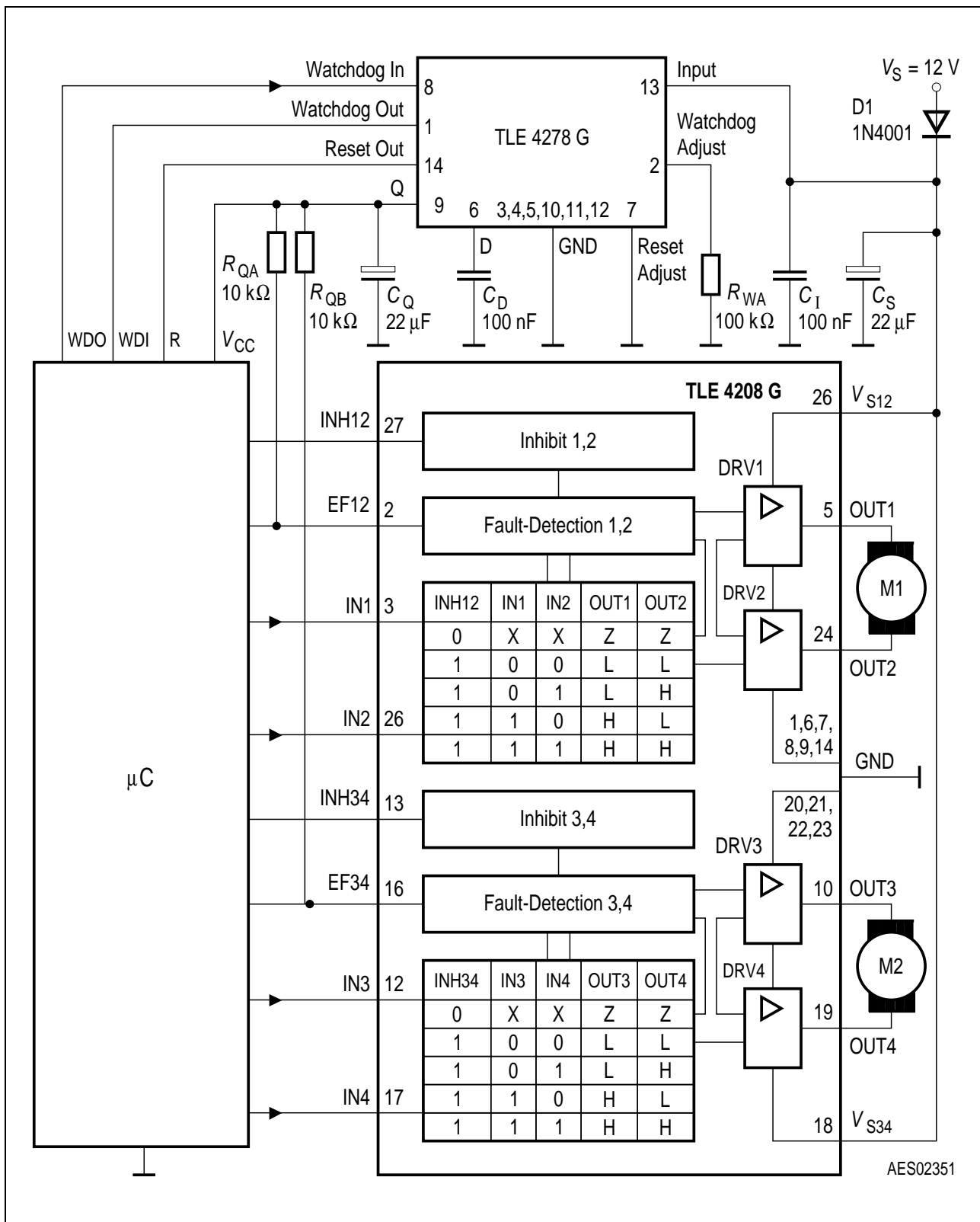
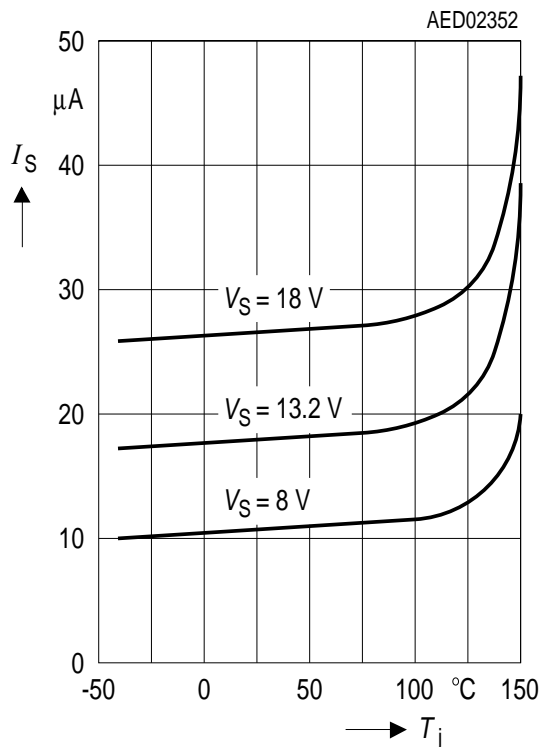


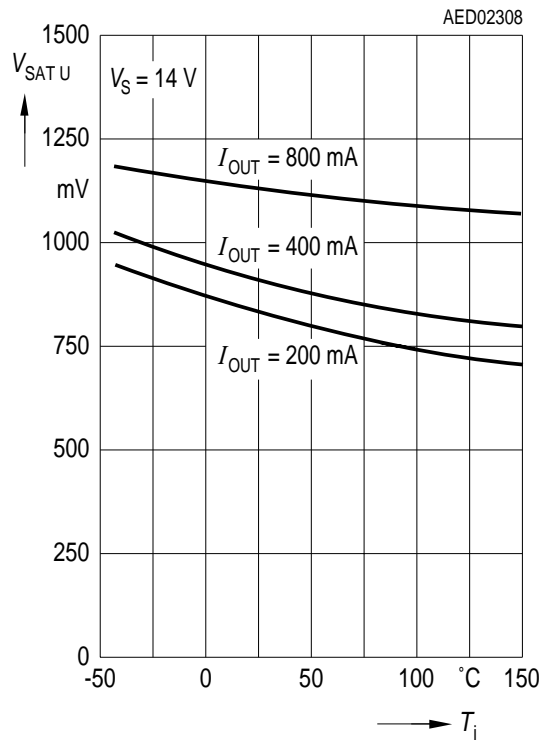
Figure 3 Application Circuit 1 (Device is Used as Dual-Full-Bridge-Driver)

Diagrams

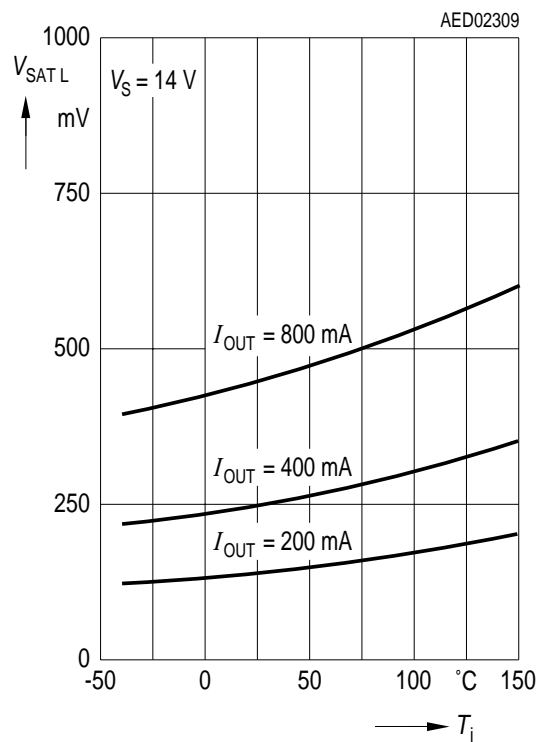
Quiescent current  $I_S$  over Temperature



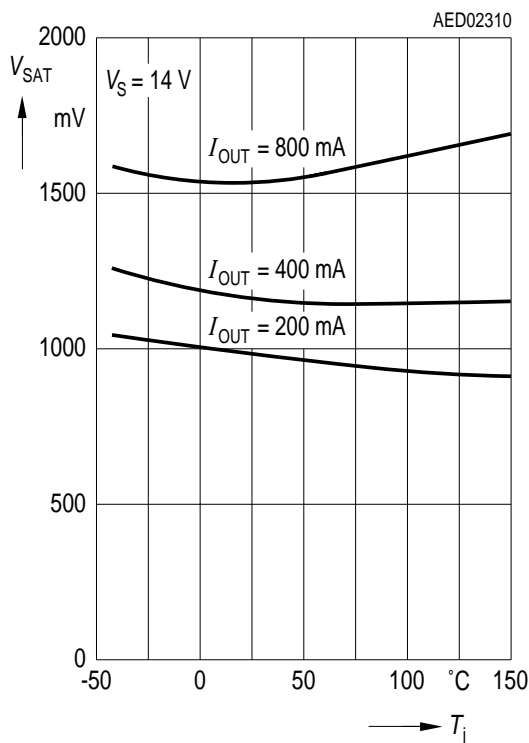
Saturation Voltage of Source  $V_{SAT U}$  over Temperature



Saturation Voltage of Sink  $V_{SAT L}$  over Temperature

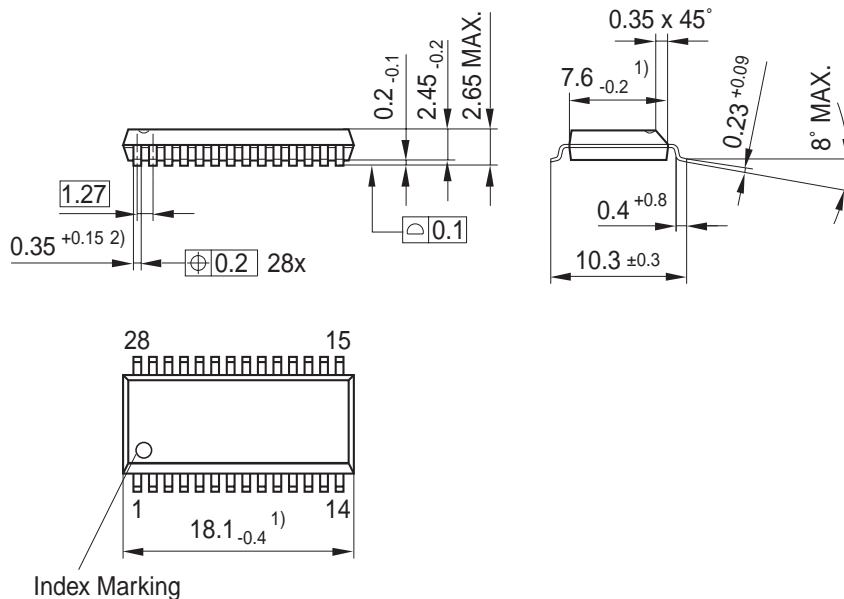


Total Drop at outputs  $V_{SAT}$  over Temperature



## Package Outlines

### P-DSO-28-18 (Plastic Dual Small Outline Package)



Index Marking

1) Does not include plastic or metal protrusion of 0.15 max. per side

2) Does not include dambar protrusion of 0.05 max. per side

### Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm