



MFM5101 Handphone Ring Tone Chip

Specification

May. 2008

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1 Overview

1.1 Introduction

MFM5101 is a highly integrated MIDI ring tones generator for handphone with high performance. A high performance Wavetable music synthesizer is integrated in this chip specifically for MIDI synthesis. A Codec used for 2/4bit ADPCM decoding, an I/O interface unit, a high performance 16 bit music DAC power amplifier and an internally configurable PLL which can receive multi-frequency clock inputs are also implemented on chip. MFM5101 can help effectively forming audio sub-system, providing high quality synthesized music and supporting stereo output.

1.2 Feature

MFM5101 synthesizes input MIDI signals via on-chip music synthesizer. It can also decode input ADPCM signals via on-chip ADPCM codec. Then it outputs analog signals through embedded DAC. MFM5101 has following features:

- **An on-chip high quality GM tone library of MIDI, capacity up to 3Mb**
- **Besides GM tone library, can also provide Chinese music instruments tone library, e.g. Urheen, Zheng, Pi-Pa etc. more than 20 Chinese music instruments**
- **Support multi-tone and chord: maximum 16 tones and 64 chords**
- **Functional I/O ports**
 - Handphone vibration drive
 - LCD back-light drive
 - PWM output which is synchronized with played music
- **Selectable interfaces**
 - 3 or 4 line modes synchronous serial interface
 - Or 8 bit width of parallel interface
- **Embedded FIFO for different input data**
- **Low power consumption, typically 50μA under standby mode; less than 80mA working current in worst case**
- **Power supply range:**
 - Core voltage: 1.7v ~ 1.9v
 - I/O, analog part and PLL voltage: 2.7v ~ 3.6v
- **Operating temperature: - 20°C ~ + 85°C**

1.3 Block Diagram

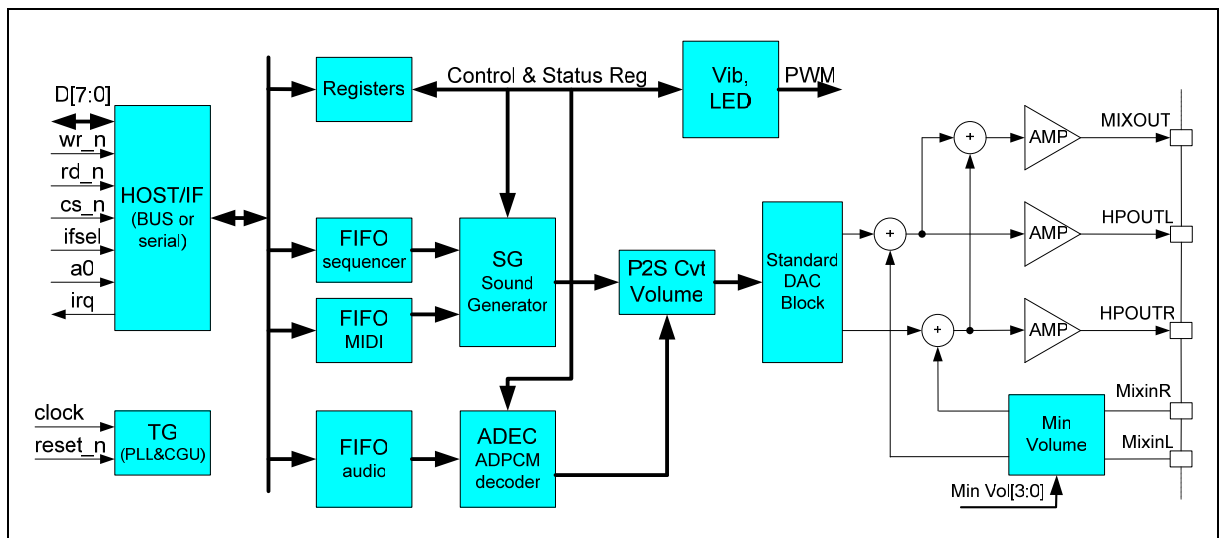


Figure 1-1 MFM5101 Block Diagram

1.4 Pin Description

Chip package could be QFN48.

Pin Name	QFN48 Pin Number	I/O	Description
A0	1	I	HOST address/data control, high for address.
IRQ	2	O	Interrupt output
IFSEL	3	I	Interface selection
RESET_N	4	I	System reset, active low
VDDP	5	PLL VDD	PLL VDD
VSSP	6	PLL GND	PLL GROUND
CLKI	7	I	System clock input, 4MHz ~ 32MHz
PWM0	8	O	PWM output
PWM1	9	O	PWM output
VIB	10	O	Handphone vibration drive
VSSIO	11	GND	I/O ground
VSSC1	12	GND	Core ground
VDDC1	13	VDD	Chip power supply VDD
LED	14	O	LED output, brightness regulatable
PWM2	15	O	PWM output
VDDIO	16	IO VDD	I/O VDD
MCLK	17	I/O	General serial DAC interface clock. Internal DAC's clock input in 'DAC in' mode.
BCLK	18	I/O	General serial DAC interface bit clock. Internal DAC's bit clock input in 'DAC in' mode.

Pin Name	QFN48 Pin Number	I/O	Description
SD0	19	I/O	General serial DAC interface data. Internal DAC's data input in 'DAC in' mode.
LRCLK	20	I/O	General serial DAC interface Left/Right channel clock. Internal DAC's Left/Right channel clock input in 'DAC in' mode.
DAC-TEST	21	I	DAC test control. Normal operation mode when low and 'DAC in' mode when high. Pull down internally.
MIXOUT	22	Analog output	Analog mixed music output
MIXNIL	23	Analog input	Analog mixed music input left channel
MIXINR	24	Analog input	Analog mixed music input right channel
VDDA	25	Analog VDD	Analog VDD
HPOUTR	26	Analog output	Earphone output, right channel
HPOUTL	27	Analog output	Earphone output, left channel
VSSA	28	Analog GND	Analog ground
VREF	29	I	Internal reference voltage, need connect to external 0.1 μ F + 4.7 μ F capacitor
D7	30	I/O	HOST data interface, output "0" in serial interface mode.
D6	31	I/O	HOST data interface, output "0" in serial interface mode.
D5/EFREQ	32	I/O	HOST data interface, EVENT FIFO data request in serial interface mode.
D4/SFREQ	33	I/O	HOST data interface, SCORE FIFO data request in serial interface mode.
D3/AFREQ	34	I/O	HOST data interface, ADPCM FIFO data request in serial interface mode.
D2/SCLK	35	I/O	HOST data interface, clock input in serial interface mode.
D1/SDOUT	36	I/O	HOST data interface, data output in serial interface mode.
D0/SDIN	37	I/O	HOST data interface, data input in serial interface mode.
VDDIO	38	IO VDD	I/O VDD
WR_N	39	I	HOST write enable
CS_N	40	I	HOST chip select
VDDC2	41	Core VDD	Core 1.8v power supply, with external 4.7 μ F + 0.1 μ F capacitor.
TMS	42	I	JTAG input
TDI	43	I	JTAG data input
TCK	44	I	JTAG clock input
TD0	45	O	JTAG data output
PD	46	I	Low power control, "1" normal mode, "0" low power mode.
VSSIO	47	IO GND	I/O ground
RD_N	48	I	HOST read enable

Table 1-1 MFM5101 Pin Description

2 Electrical Parameters

2.1 Maximum Ratings

Parameters	2.1.1.1 Symbol	Condition	Range	Unit
Power supply	VDDC	Ta = 25C	-0.3 ~ + 2.0	V
	VDDA, VDDP, VDDIO		-0.3 ~ + 3.6	V
Input voltage	Vin		-0.3 ~ VDDIO + 0.3	V
Power consumption	Pd		400	mW
Storage temperature	Tstg	-	-55 ~ +125	°C

Table 2-1 MFM5101 Maximum Ratings

2.2 Recommended Operating Conditions

Symbol	Parameters	Condition	MIN	TYP	MAX	Unit
VDDC	Power supply for digital portion	VSSC = VSSIO = VSSA = VSSP = 0V	1.7	1.8	1.9	V
VDDA	Power supply for analog portion	VSSC = VSSIO = VSSA = VSSP = 0V	2.7	3.0	3.6	V
VDDIO	IO power supply	VSSC = VSSIO = VSSA = VSSP = 0V	2.7	3.0	3.6	V
Top	Operating temperature	-	- 20	+ 25	+ 85	°C
fclock	Input clock frequency	-	4	13	32	MHz

Table 2-2 MFM5101 Recommended Operating Conditions

2.3 DC Electrical Characteristics

Applicable over recommended operating range from: VDDC = 1.8V, VDDA = VDDP = VDDIO = 3.0V, Ta = 25°C (unless otherwise noted)

Symbol	Parameters	Condition	MIN	TYP	MAX	Unit
V _{IL}	Input low voltage	-	-	-	VDDIO*0.2	V
V _{IH}	Input high voltage	-	VDDIO*0.8	-	-	V
V _{IL2}	CLKI Input low voltage	-	-	0	0.2	V
V _{IH2}	CLKI Input high voltage	-	-	VDDIO	-	V
I _{IL}	Input Low Leakage	V _{IL} =VDDIO	-1	0.1	-	μA
I _{IH}	Input High Leakage	V _{IH} =VSSIO	-	0.1	1	μA
V _{OL}	Output low voltage	I _{ol} =2mA	-	-	VDDIO*0.2	V
V _{OH}	Output high voltage	I _{oh} =2mA	VDDIO*0.8	-	-	V
V _{OL3}	VIB pin output low voltage	I _{OL3} =100mA	-	-	0.60	V
V _{OL4}	LED pin output low voltage	I _{OL4} =16mA	-	-	0.45	V
I _{dd}	Operating current	Stereo earphone outputs, and analog parts works	-	60	80 ⁽¹⁾	mA
I _{dds}	Standby current	Room temperature 25°C	-	30	100 ⁽²⁾	μA

Table 2-3 MFM5101 DC Electrical Characteristics

Note: 1. Test condition: Ta = 85°C, VDDA = VDDIO = VDDP = 3.6V, VDDC = 1.9V.

2. Test condition: Ta = 85°C, VDDA = VDDIO = VDDP = 3.6V, VDDC = 1.9V.

2.4 DAC Characteristics

Applicable over recommended operating range from: VDDC = 1.8V, VDDA = VDDP = VDDIO = 3.0V, Ta = 25°C (unless otherwise noted)

Symbol	Parameters	Condition	MIN	TYP	MAX	Unit
Fs	Sampling frequency	-	-	48	-	KHz
B	Resolution	-	-	16	-	Bit
THD	Harmonic distortion & noisy	Signal Frequency: 1KHz	-	0.025% -72db	-	
PSRR	Power suppression ratio (200Hz ~ 1KHz)	Noise band: 200Hz ~ 1KHz No load	40	50	-	dB
CS	Channel Separation	Signal Frequency : 1KHz No load	-	-	-55	dB
HP Vp-p	HPOUT Output Peak to Peak	32Ω AC load DAC Volume: -2dB	1.2	1.4	-	Vp-p
MIX Vp-p	MIXOUT OUTPUT Peak to Peak	10KΩ AC load DAC Volume: -2dB	1.2	1.4	-	Vp-p
THD _{MP}	THD between MIXIN and HPOUT	RI=32Ω/ f=1KHz Vout= - 6dB	-	-57	-	dB
THD _{MM}	THD between MIXIN and MIXOUT	RI=10KΩ/ f=1KHz Vout= - 6dB	-	-60	-	dB

Table 2-4 MFM5101 DAC Parameters

3 Typical Application Circuit

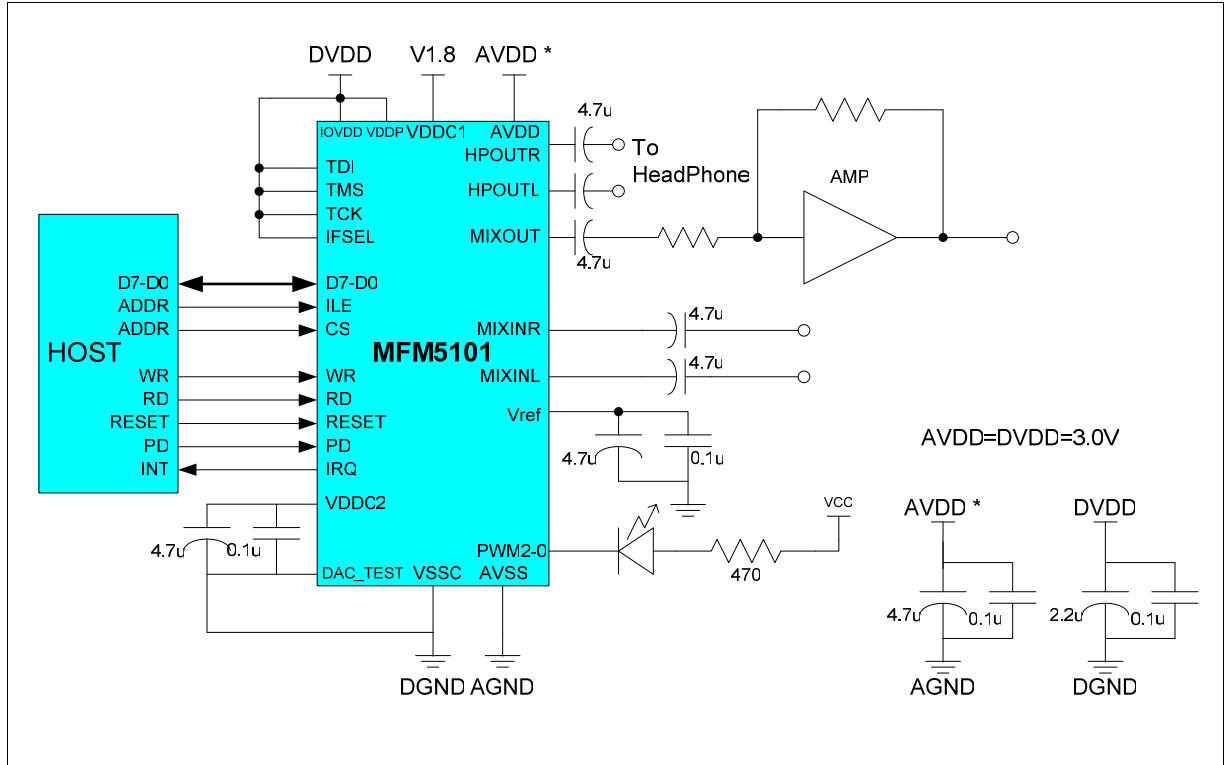


Figure 3-1 MFM5101 Typical Application Circuit

4 Package Dimensions

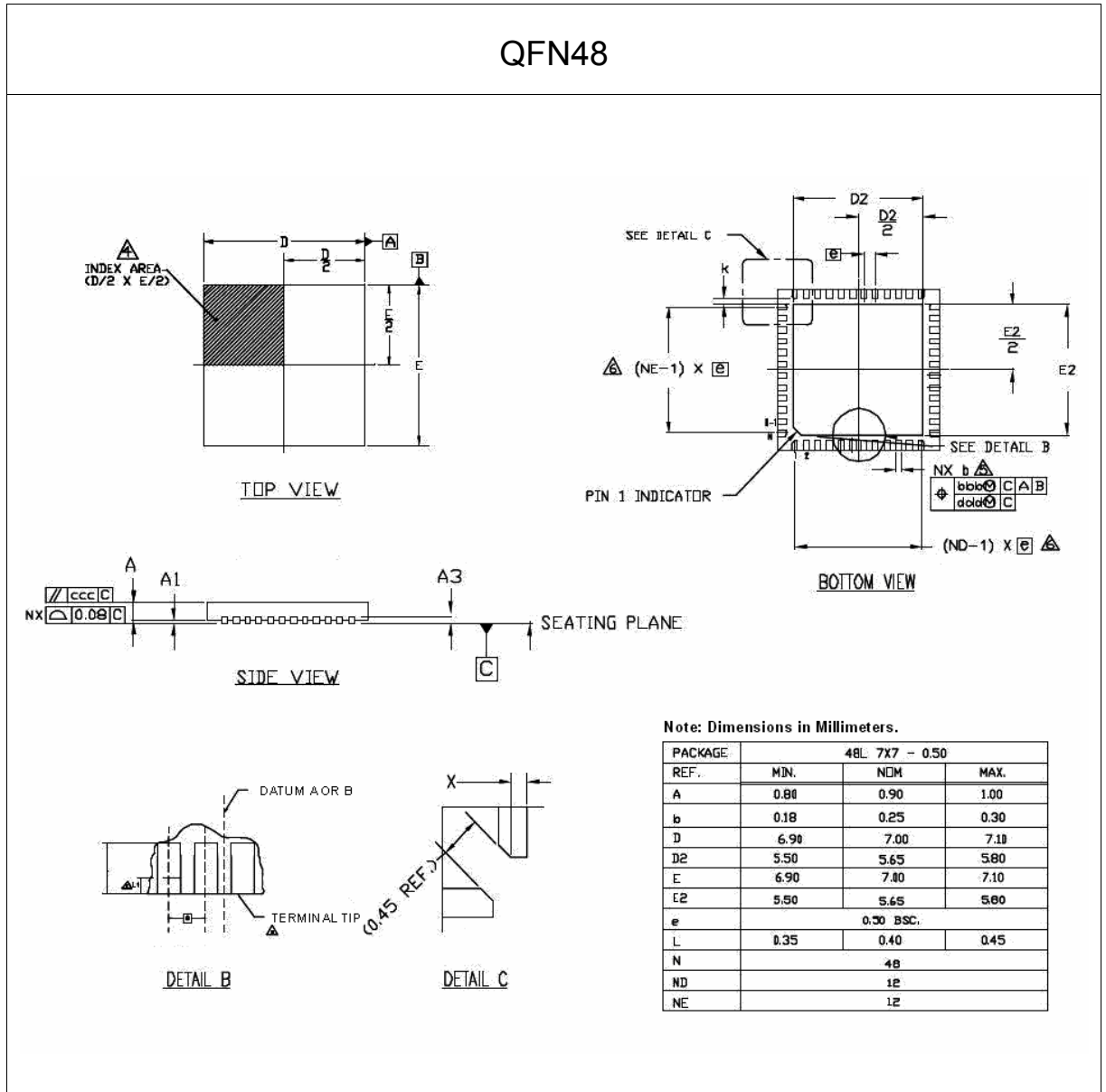


Figure 4-1 MFM5101 QFN48 Package Dimensions

Note: The figure is only for illustration and in fact there are 12 PINs per side on the base.

5 Ordering Information

Ordering Code	Package	Operation Range
MFM5101-QFN (R) ⁽¹⁾	QFN48 (R)	Industrial Temperature -20°C ~ +85°C

Note: 1. The “R” denotes: RoHS compliant.

6 Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
1.0	Mar. 2007	13		Initial Release.
2.0	Oct. 2007	13		Updated Format.
2.1	May. 2008	13	Sales and service	Updated the address of HK office.

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