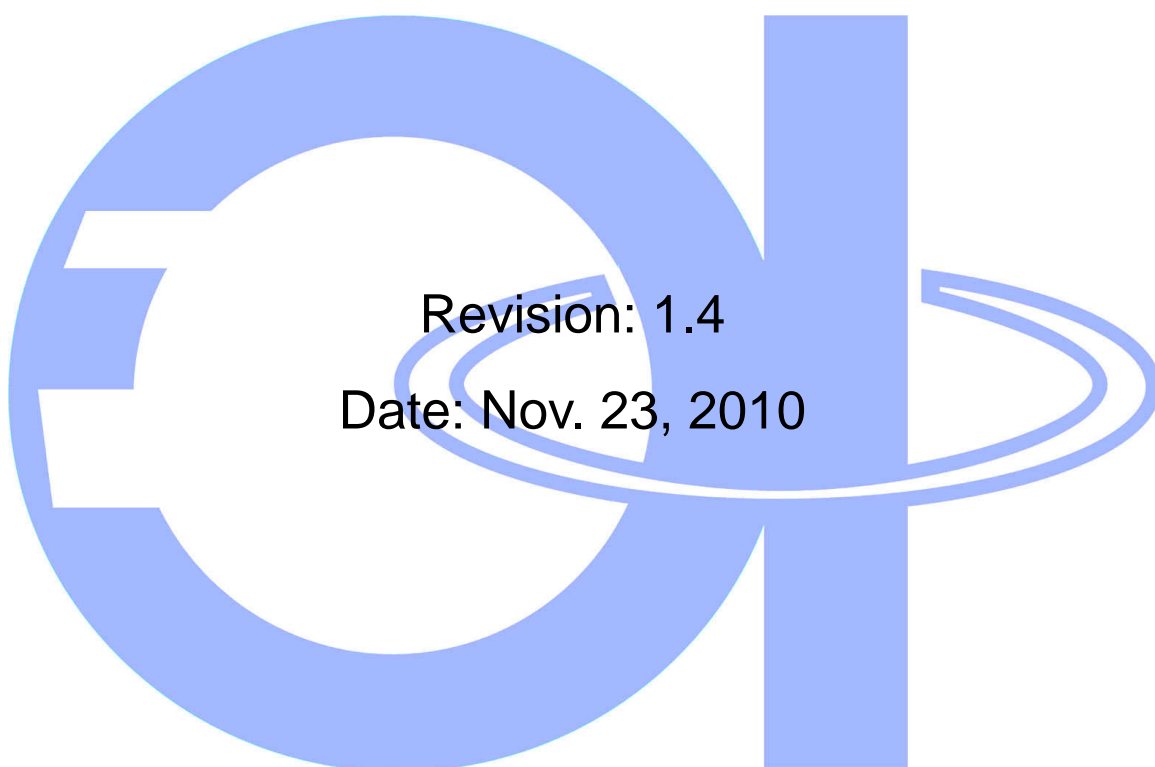


# **JL4203A**

## ***Multimedia Controller***



Revision: 1.4

Date: Nov. 23, 2010

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## 0. Revision History

Revision	Description of Changes	Date
1.0	First Formal Release	2007/09/27
1.1	<ol style="list-style-type: none"><li>1. Update pin name.</li><li>2. Update block diagram.</li><li>3. Add AC Timing Specification.</li></ol>	2007/12/31
1.2	<ol style="list-style-type: none"><li>1. Change the video frame rate to "up to VGA@30fps".</li><li>2. Rename pin 54 to USB_REF.</li><li>3. Modify block diagram in chapter 3.</li><li>4. Modify the diagram in chapter 5.1.</li><li>5. Correct the dimension in PQFP-208 package.</li><li>6. Add Chapter 9 CHIP REVISION HISTORY.</li><li>7. Change ordering information of JL4203A to JL4203A-V2.</li></ol>	2008/05/14
1.3	<ol style="list-style-type: none"><li>1. Remove following display features in paragraph 2.<ul style="list-style-type: none"><li>● RGB565/666/888 formats</li><li>● Smaller size TFT-LCD panel with CPU interface</li></ul></li><li>2. Remove paragraph 5.4, "DDI (Digital Display Interface) Table".</li><li>3. Remove paragraph 5.5, "NAND Flash and IDE Mux Table".</li></ol>	2008/05/28



## 1. General Description

JL4203A is a multi-media system on chip (SoC) designed and developed by Jeilin Technology, Taiwan. With LCD of different size, JL4203A can be applied to make digital photo frame. Jeilin Technology will provide complete system design to allow client or distributor enter easier and earlier the digital photo frame market.

JL4203A digital photo frame can play back photos (JPEG), movie (Motion JPEG), and music (MP3) from memory card or built-in memory. This will allow user to directly view and share photos and listen to music without developing the photos for viewing later. JL4203A digital photo frame has added many functions that traditional photo frame does not have, for example, auto slide browsing, music playing in the background while photo browsing, transition effects while photo browsing, clock, alarm clock, and calendar. All these functions can be achieved without using a computer.

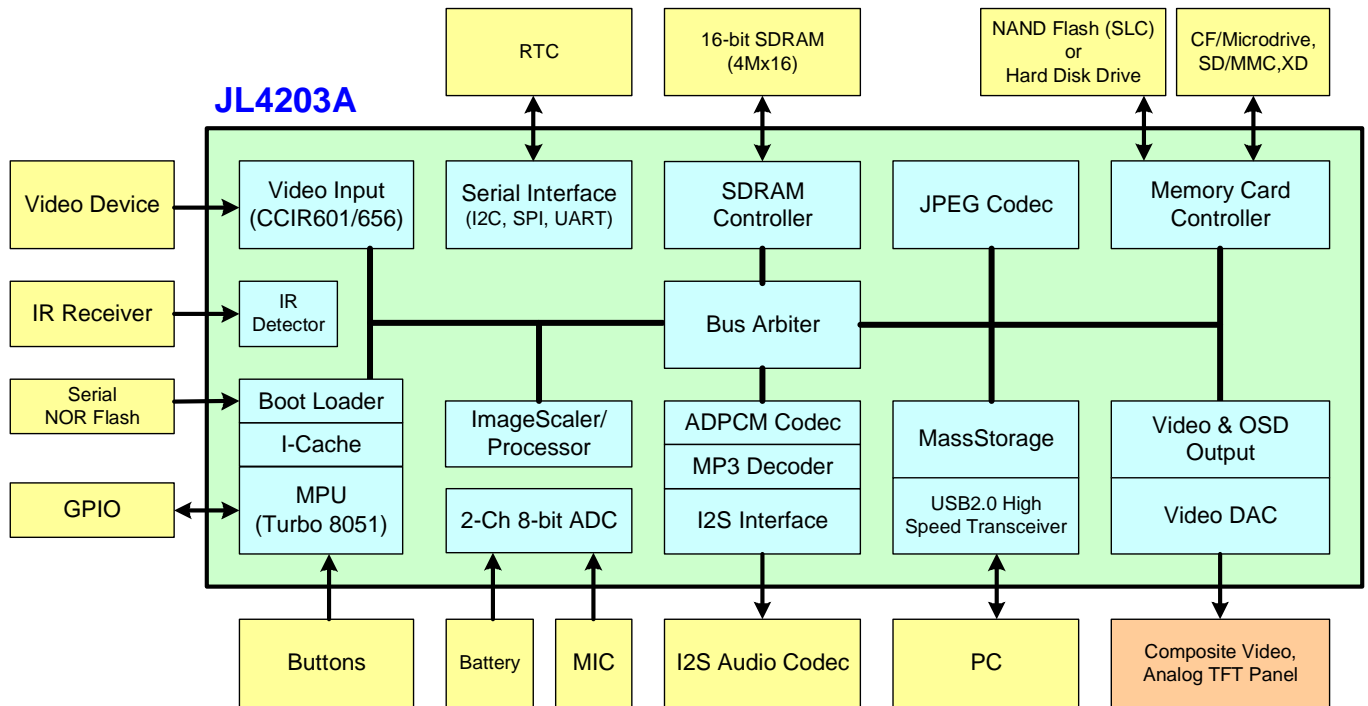
## 2. Features

- USB Interface
  - High-speed USB 2.0 device function with embedded PHY
  - Supports Mass-Storage Class (MSC)
  - Supports PictBridge interface (direct picture print)
- Storage Media
  - CompactFlash Interface
    - Complies with CF+ and CompactFlash Specification Revision 3.0
  - IDE Interface
    - ◆ Complies with ATA /ATAPI-6 Specification Rev 2.0
    - ◆ Supports PIO mode 0~4, Multiword DMA mode 0~2, and Ultra DMA mode 0~5
  - SD/MMC Interface
    - ◆ Complies with SD 2.0
    - ◆ Complies with MMC 4.0
  - NAND Flash/XD/SmartMedia Interface
- Display Feature
  - Embedded four 10-bit video DACs: one for TV display and three for analog LCD panel.
  - Embedded TV Encoder (NTSC/PAL) to output CVBS (Composite Video).
  - Supports analog RGB TFT-LCD panel
  - Supports 8-bit CCIR601/656 input and output interfaces
- OSD Feature
  - Font-based OSD
  - Graphic-based OSD



- Audio Feature
  - 8/16-bit PCM, 4-bit IMA-ADPCM audio codec
  - AC97/I<sup>2</sup>S interface
  - Embedded 2 channels of 8-bit ADC for voice record and battery detect
- MP3 Feature
  - Built-in MP3 decoder engine
  - Supports both ISO 11172-3 and ISO 13818-3 layer III audio decoding
  - Supports 8 KHz, 11.025 KHz, 12 KHz, 16 KHz, 22.05 KHz, 24 KHz, 32 KHz, 44.1 KHz, 48 KHz sampling rate
  - Ten-band equalizer with 64 steps for -20 to 20 dB gain.
  - Photo slide show with MP3 background playback.
- JPEG codec
  - Supports photo resolution up to 16,384 x 16,384 pixels
  - High-speed JPEG compression/decompression rate: 27 Mega pixels per second
  - Supports non-progressive JPEG
  - Supports baseline JPEG format
  - Supports thumbnail decoding
- Video Playback
  - File Format : Only Support Motion JPEG
  - Audio Signal : PCM Format 、ADPCM Format
  - Video Frame Rate : up to VGA@30fps
  - Supports video scaling and Picture-In-Picture functions
- SDRAM interface
  - Supports 16-bit SDRAM up to 8Mx16 bits
- Image Display Functions
  - Preview, Slide Show, Zoom, Pan, Rotate, and so on
  - Image Rotation: 0, 90, 180, or 270 degree in clockwise or counter-clockwise direction
  - Image scale function to fit screen
  - Picture In Picture display
  - Transition Effect in photo playback
- Embedded Turbo 8051
  - Supports ISP Function: It is easy-to-use function to upgrade the system firmware directly from memory cards.
  - Provides lots of GPIOs
- Provides UART, SPI-master and I<sup>2</sup>C-master serial ports
- Package : 208-pin PQFP

### 3. Block Diagram



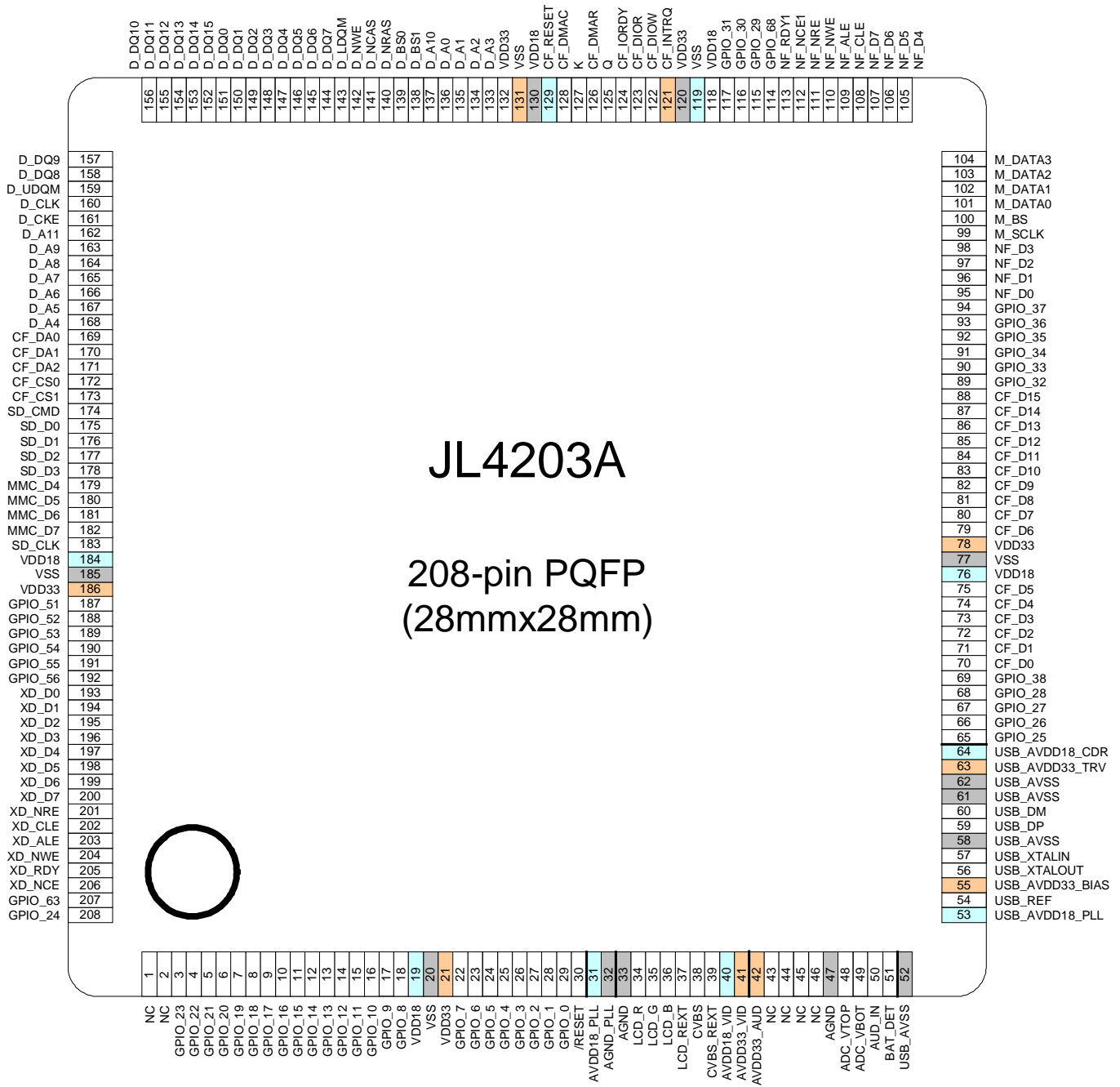
### 4. Applications

- Digital Photo Frame (DPF)
  - Viewing Photos (JPEG)
  - Viewing Movie (Motion JPEG AVI)
  - Listening to MP3 music
- USB2.0 Card Reader
- DPF with Clock/Calendar



### 5. Pin Assignment and Pin Description

#### 5.1 Pin Assignment





## 5.2 Pin Description

Pin #	Pin name	Type	Description	Memo
1	NC		Reserved pin	
2	NC		Reserved pin	
3	GPIO_23	B2	General purpose I/O #23	DDI_23
4	GPIO_22	B2	General purpose I/O #22	DDI_22
5	GPIO_21	B2	General purpose I/O #21	DDI_21
6	GPIO_20	B2	General purpose I/O #20	DDI_20
7	GPIO_19	B2	General purpose I/O #19	DDI_19
8	GPIO_18	B2	General purpose I/O #18	DDI_18
9	GPIO_17	B2	General purpose I/O #17	DDI_17
10	GPIO_16	B2	General purpose I/O #16	DDI_16
11	GPIO_15	B2	General purpose I/O #15	DDI_15
12	GPIO_14	B2	General purpose I/O #14	DDI_14
13	GPIO_13	B2	General purpose I/O #13	DDI_13
14	GPIO_12	B2	General purpose I/O #12	DDI_12
15	GPIO_11	B2	General purpose I/O #11	DDI_11
16	GPIO_10	B2	General purpose I/O #10	DDI_10
17	GPIO_9	B2	General purpose I/O #9	DDI_9
18	GPIO_8	B2	General purpose I/O #8	DDI_8
19	VDD18	P	Core power 1.8V	
20	VSS	G	Ground	
21	VDD33	P	Pad power 3.3V	
22	GPIO_7	B2	General purpose I/O #7	DDI_7
23	GPIO_6	B2	General purpose I/O #6	DDI_6
24	GPIO_5	B2	General purpose I/O #5	DDI_5
25	GPIO_4	B2	General purpose I/O #4	DDI_4
26	GPIO_3	B2	General purpose I/O #3	DDI_3
27	GPIO_2	B4	General purpose I/O #2	DDI_2
28	GPIO_1	B4	General purpose I/O #1	DDI_1
29	GPIO_0	B4	General purpose I/O #0	DDI_0
30	/RESET	B2	Reserved pin, which must be pull-high with a 10K ohms resistor	
31	AVDD18_PLL	P	PLL power 1.8V	
32	AGND_PLL	G	PLL ground	
33	AGND	G	Analog ground	





Pin #	Pin name	Type	Description	Memo
34	LCD_R	A	R channel analog output signal	
35	LCD_G	A	G channel analog output signal	
36	LCD_B	A	B channel analog output signal	
37	LCD_REXT	A	The reference current for the video DAC. This pin should connect a resistor to ground. The output current $I = 128 * 1.25 / R_{ext}$ (mA)	
38	CVBS	A	Composite video signal output	
39	CVBS_REXT	A	The reference current for the video DAC. This pin should connect a resistor to ground. The output current $I = 128 * 1.25 / R_{ext}$ (mA)	
40	AVDD18_VID	P	Video DAC power 1.8V	
41	AVDD33_VID	P	Video DAC power 3.3V	
42	AVDD33_AUD	P	ADC/DAC power 3.3V	
43	NC	A	Reserved pin	
44	NC	A	Reserved pin	
45	NC	A	Reserved pin	
46	NC	A	Reserved pin	
47	AGND	G	Analog ground	
48	ADC_VTOP	A	Reference voltage decoupling for audio ADC. The nominal value is 2.7V. It should be connected an 0.1uF capacitor to ground	
49	ADC_VBOT	A	Reference voltage decoupling for audio ADC. The nominal value is 1.2V. It should be connected an 0.1uF capacitor to ground	
50	AUD_IN	A	Audio signal input	
51	BAT_DET	A	Battery voltage detect input	
52	USB_AVSS	G	USB PHY ground	
53	USB_AVDD18_PLL	P	USB PLL power 1.8V	
54	USB_REF	A	Connect 12.1Kohm (1%) resistor to ground. The purpose of RES is to provide a reference for the current resource of the high-speed driver.	
55	USB_AVDD33_BIAS	P	3.3V power for BIAS	
56	USB_XTALOUT	A	Oscillator output. Connect to a 12Mhz crystal	
57	USB_XTALIN	A	Oscillator input. Connect to a 12Mhz crystal	
58	USB_AVSS	G	USB PHY ground	



Pin #	Pin name	Type	Description	Memo
59	USB_DP	A	USB D+	
60	USB_DM	A	USB D-	
61	USB_AVSS	G	USB PHY ground	
62	USB_AVSS	G	USB PHY ground	
63	USB_AVDD33_TRV	P	3.3V power for USB transceiver	
64	USB_AVDD18_CDR	P	1.8V power for CDR	
65	GPIO_25	B2	General purpose I/O #25	
66	GPIO_26	B2	General purpose I/O #26	
67	GPIO_27	B2	General purpose I/O #27	
68	GPIO_28	B2	General purpose I/O #28	
69	GPIO_38	B2	General purpose I/O #38	
70	CF_D0	B4	CF data bus 0	
71	CF_D1	B4	CF data bus 1	
72	CF_D2	B4	CF data bus 2	
73	CF_D3	B4	CF data bus 3	
74	CF_D4	B4	CF data bus 4	
75	CF_D5	B4	CF data bus 5	
76	VDD18	P	Core power 1.8V	
77	VSS	G	Ground	
78	VDD33	P	Pad power 3.3V	
79	CF_D6	B4	CF data bus 6	
80	CF_D7	B4	CF data bus 7	
81	CF_D8	B4	CF data bus 8	
82	CF_D9	B4	CF data bus 9	
83	CF_D10	B4	CF data bus 10	
84	CF_D11	B4	CF data bus 11	
85	CF_D12	B4	CF data bus 12	
86	CF_D13	B4	CF data bus 13	
87	CF_D14	B4	CF data bus 14	
88	CF_D15	B4	CF data bus 15	
89	GPIO_32	B2	General purpose I/O #32	
90	GPIO_33	B2	General purpose I/O #33	
91	GPIO_34	B2	General purpose I/O #34	
92	GPIO_35	B2	General purpose I/O #35	
93	GPIO_36	B2	General purpose I/O #36	



Pin #	Pin name	Type	Description	Memo
94	GPIO_37	B2	General purpose I/O #37	
95	NF_D0	B4	Data 0 of NAND Flash memory	
96	NF_D1	B4	Data 1 of NAND Flash memory	
97	NF_D2	B4	Data 2 of NAND Flash memory	
98	NF_D3	B4	Data 3 of NAND Flash memory	
99	M_SCLK	O8	Memory Clock Output	GPIO_57
100	M_BS	O4	Memory Bus State Output	GPIO_58
101	M_DATA0	B4	Memory Parallel Data Line 0.	GPIO_59
102	M_DATA1	B4	Memory Parallel Data Line 1.	GPIO_60
103	M_DATA2	B4	Memory Parallel Data Line 2.	GPIO_61
104	M_DATA3	B4	Memory Parallel Data Line 3.	GPIO_62
105	NF_D4	B4	Data 4 of NAND Flash memory	
106	NF_D5	B4	Data 5 of NAND Flash memory	
107	NF_D6	B4	Data 6 of NAND Flash memory	
108	NF_D7	B4	Data 7 of NAND Flash memory	
109	NF_CLE	O4	Command latch enable for NAND Flash memory	
110	NF_ALE	O4	Address latch enable for NAND Flash memory	
111	NF_NWE	O4	Write strobe for NAND Flash memory	
112	NF_NRE	O4	Read strobe for NAND Flash memory	
113	NF_NCE1	O16	Chip enable signal for the 1 <sup>st</sup> die on NAND Flash	
114	NF_RDY1	I	Ready signal of the 1 <sup>st</sup> die on NAND Flash	
115	GPIO_68	B2	General purpose I/O #68	
116	GPIO_29	B2	General purpose I/O #29	
117	GPIO_30	B2	General purpose I/O #30	
118	GPIO_31	B2	General purpose I/O #31	
119	VDD18	P	Core power 1.8V	
120	VSS	G	Ground	
121	VDD33	P	Pad power 3.3V	
122	CF_INTRQ	I	CF Interrupt Request	
123	CF_DIOW	O4	CF read strobe output	
124	CF_DIOR	O4	CF write strobe output	
125	CF_IORDY	I	CF card ready	
126	CF_DMARQ	O4	DMA acknowledge signal in true IDE mode.	
127	CF_DMACK	O4	DMA request signal in true IDE mode.	
128	CF_RESET	O4	Hardware Reset output	



Pin #	Pin name	Type	Description	Memo
129	VDD18	P	Core power 1.8V	
130	VSS	G	Ground	
131	VDD33	P	Pad power 3.3V	
132	D_A3	O8	SDRAM address bus 3, which must be pull-high with a 10K ohm resistor for normal operation	
133	D_A2	O8	SDRAM address bus 2, which must be pull-high with a 10K ohm resistor for normal operation	
134	D_A1	O8	SDRAM address bus 1	* Note 1
135	D_A0	O8	SDRAM address bus 0	* Note 1
136	D_A10	O8	SDRAM address bus 10	
137	D_BS1	O8	SDRAM bank address 1	
138	D_BS0	O8	SDRAM bank address 0	
139	D_NRAS	O8	SDRAM row address strobe output	
140	D_NCAS	O8	SDRAM column address strobe output	
141	D_NWE	O8	SDRAM write strobe	
142	D_LDQM	O8	SDRAM low byte data write mask	
143	D_DQ7	B8	SDRAM data bus 7	
144	D_DQ6	B8	SDRAM data bus 6	
145	D_DQ5	B8	SDRAM data bus 5	
146	D_DQ4	B8	SDRAM data bus 4	
147	D_DQ3	B8	SDRAM data bus 3	
148	D_DQ2	B8	SDRAM data bus 2	
149	D_DQ1	B8	SDRAM data bus 1	
150	D_DQ0	B8	SDRAM data bus 0	
151	D_DQ15	B8	SDRAM data bus 15	
152	D_DQ14	B8	SDRAM data bus 14	
153	D_DQ13	B8	SDRAM data bus 13	
154	D_DQ12	B8	SDRAM data bus 12	
155	D_DQ11	B8	SDRAM data bus 11	
156	D_DQ10	B8	SDRAM data bus 10	
157	D_DQ9	B8	SDRAM data bus 9	
158	D_DQ8	B8	SDRAM data bus 8	
159	D_UDQM	O8	SDRAM high byte data write mask	
160	D_CLK	O8	SDRAM clock	
161	D_CKE	O8	SDRAM clock enable	



Pin #	Pin name	Type	Description	Memo
162	D_A11	O8	SDRAM address bus 11	
163	D_A9	O8	SDRAM address bus 9	
164	D_A8	O8	SDRAM address bus 8	
165	D_A7	O8	SDRAM address bus 7	
166	D_A6	O8	SDRAM address bus 6	
167	D_A5	O8	SDRAM address bus 5	
168	D_A4	O8	SDRAM address bus 4	
169	CF_DA0	O4	CF Address Line 0	
170	CF_DA1	O4	CF Address Line 1	
171	CF_DA2	O4	CF Address Line 2	
172	CF_CS0	O4	CF Chip Select 0 in true IDE mode	
173	CF_CS1	O4	CF Chip Select 1 in true IDE mode	
174	SD_CMD	B4	Command signal for SD/MMC	GPIO_42
175	SD_D0	B4	Data bit 0 of SD/MMC	GPIO_43
176	SD_D1	B4	Data bit 1 of SD/MMC	GPIO_44
177	SD_D2	B4	Data bit 2 of SD/MMC	GPIO_45
178	SD_D3	B4	Data bit 3 of SD/MMC	GPIO_46
179	MMC_D4	B4	Data bit 4 of MMC	GPIO_47
180	MMC_D5	B4	Data bit 5 of MMC	GPIO_48
181	MMC_D6	B4	Data bit 6 of MMC	GPIO_49
182	MMC_D7	B4	Data bit 7 of MMC	GPIO_50
183	SD_CLK	O8	Clock signal for SD/MMC	GPIO_41
184	VDD18	P	Core power 1.8V	
185	VSS	G	Ground	
186	VDD33	P	Pad power 3.3V	
187	GPIO_51	B2	General purpose I/O #51	
188	GPIO_52	B2	General purpose I/O #52	
189	GPIO_53	B2	General purpose I/O #53	
190	GPIO_54	B2	General purpose I/O #54	
191	GPIO_55	B2	General purpose I/O #55	
192	GPIO_56	B2	General purpose I/O #56	
193	XD_D0	B4	Data bit 0 of XD	
194	XD_D1	B4	Data bit 1 of XD	
195	XD_D2	B4	Data bit 2 of XD	
196	XD_D3	B4	Data bit 3 of XD	



Pin #	Pin name	Type	Description	Memo
197	XD_D4	B4	Data bit 4 of XD	
198	XD_D5	B4	Data bit 5 of XD	
199	XD_D6	B4	Data bit 6 of XD	
200	XD_D7	B4	Data bit 7 of XD	
201	XD_NRE	O4	Read strobe for XD	
202	XD_CLE	O4	Command latch enable for XD	
203	XD_ALE	O4	Address latch enable for XD	
204	XD_NWE	O4	Write strobe for XD	
205	XD_RDY	O4	Ready signal for XD	
206	XD_NCE	O4	Chip enable signal for XD	
207	GPIO_63	B16	General purpose I/O # 63	
208	GPIO_24	B2	General purpose I/O # 24	DDI_24



## NOTE:

\*1: Pull up/down these two pins with 10K ohm resistor to select system booting method.

Booting Mode	Function
00	Booting from iROM
01	Booting from Serial NOR Flash
10	Reserved
11	Reserved

\*2: All digital input pin can take 5V tolerance

Type	Description
P	Power pin
G	Ground pin
A	Analog pin
I	3.3V CMOS input pin
O4	3.3V CMOS output pin with 4mA driving ability
O8	3.3V CMOS output pin with 8mA driving ability
O24	3.3V CMOS output pin with 24mA driving ability
B	3.3V CMOS bi-direction pin with 2mA driving ability
B4	3.3V CMOS bi-direction pin with 4mA driving ability
B8	3.3V CMOS bi-direction pin with 8mA driving ability
B16	3.3V CMOS bi-direction pin with 16mA driving ability
OD	3.3V CMOS open drain output pin



**5.3 GPIO Mux Table:**

NOTE: Each GPIO pin has its own function select registers, Alt[2:1], firmware can configure each GPIO pin to different function individually.

Alt[2:1]= 00		Alt[2:1]= 01		Alt[2:1]= 10		Alt[2:1]= 11	
GPIO_0	B	DDI_0	O	-		-	
GPIO_1	B	DDI_1	O	-		-	
GPIO_2	B	DDI_2	O	-		-	
GPIO_3	B	DDI_3	O	-		-	
GPIO_4	B	DDI_4	O	-		-	
GPIO_5	B	DDI_5	O	-		-	
GPIO_6	B	DDI_6	O	-		-	
GPIO_7	B	DDI_7	O	-		-	
GPIO_8	B	DDI_8	O	-		-	
GPIO_9	B	DDI_9	O	-		-	
GPIO_10	B	DDI_10	O	-		-	
GPIO_11	B	DDI_11	O	CCIR601_In_CLK	I	-	
GPIO_12	B	DDI_12	O	CCIR601_In_D0	I	-	
GPIO_13	B	DDI_13	O	CCIR601_In_D1	I	-	
GPIO_14	B	DDI_14	O	CCIR601_In_D2	I	-	
GPIO_15	B	DDI_15	O	CCIR601_In_D3	I	-	
GPIO_16	B	DDI_16	O	CCIR601_In_D4	I	-	
GPIO_17	B	DDI_17	O	CCIR601_In_D5	I	-	
GPIO_18	B	DDI_18	O	CCIR601_In_D6	I	UART_TX	O
GPIO_19	B	DDI_19	O	CCIR601_In_D7	I	UART_RX	I
GPIO_20	B	DDI_20	O	CCIR601_In_HSYNC	I	-	
GPIO_21	B	DDI_21	O	CCIR601_In_VSYNC	I	-	
GPIO_22	B	DDI_22	O	-		-	
GPIO_23	B	DDI_23	O	-		-	
GPIO_24	B	DDI_24	O	-		-	
GPIO_25	B	I2S_PWDN		AC_Link_nReset	O	-	
GPIO_26	B	I2S_WS	O	AC_Link_Sync	O	-	
GPIO_27	B	I2S_BCK	O	AC_Link_BClk	I	-	
GPIO_28	B	I2S_DATAO	O	AC_Link_SDataOut	O	-	
GPIO_29	B	SCL	OD	-		-	
GPIO_30	B	SDA	OD	-		-	
GPIO_31	B	AC_Link_SDataIn	I	PG1_Out_1	O	-	





Alt[2:1]= 00		Alt[2:1]= 01		Alt[2:1]= 10		Alt[2:1]= 11	
GPIO_32	B	IR_In_0	I	-		-	
GPIO_33	B	SPI_nCS_1	O	PWM Signal Output	O	-	
GPIO_34	B	SPI_nCS_0	O	ROM_NCS	O	-	
GPIO_35	B	SPI_SCK	O	-		-	
GPIO_36	B	SPI_DO	O	UART_TX	O	-	
GPIO_37	B	SPI_DI	I	UART_RX	I	-	
GPIO_38	B	AC_Link_SDataIn	I	PG1_Out_1	O	-	
GPIO_39	B	NF_nCE1	O	-		-	
GPIO_40	B	NF_RDY1	I	PWM Signal Output	O	-	
GPIO_41	B	SD_CLK	O	-		-	
GPIO_42	B	SD_CMD	O	-		-	
GPIO_43	B	SD_D0	B	-		-	
GPIO_44	B	SD_D1	B	-		-	
GPIO_45	B	SD_D2	B	-		-	
GPIO_46	B	SD_D3	B	-		-	
GPIO_47	B	SD_D4	B	-		-	
GPIO_48	B	SD_D5	B	-		-	
GPIO_49	B	SD_D6	B	-		-	
GPIO_50	B	SD_D7	B	-		-	
GPIO_51	B	-		NF_nCE2	O	-	
GPIO_52	B	-		NF_RDY2	I	Ext_Clk_Out	O
GPIO_53	B	-		NF_nCE3	O	-	
GPIO_54	B	-		NF_RDY3	I	DDI_25	O
GPIO_55	B	-		NF_nCE4	O	DDI_26	O
GPIO_56	B	-		NF_RDY4	I	DDI_27	O
GPIO_57	B	M_SCLK	O	-		-	
GPIO_58	B	M_BS	O	-		-	
GPIO_59	B	M_DATA0	B	-		-	
GPIO_60	B	M_DATA1	B	-		-	
GPIO_61	B	M_DATA2	B	-		-	
GPIO_62	B	M_DATA3	B	-		-	
GPIO_63	B	PG1_Out_1	O	-		-	
GPIO_68	B	-		-		-	

## 6. AC Characteristics

### 6.1 Serial Peripheral Interface

- SPI mode 0

Symbol	Parameter	Min.	Max.	Unit
tCISh	-CS low to SCK high	-	230	ns
tShCh	SCK high to -CS high	-	125	ns
tCRT	Clock Rise Time	0.1	-	V/ns
tCFT	Clock Fall Time	0.1	-	V/ns
tSU:DAT	Data in Setup Time	10	-	ns
tHD:DAT	Data in Hold Time	5	-	ns
tV	Output Valid	-	5	ns
tHO	Output Hold Time	-	5	ns
tWH	SCK High Time	-	35	ns
tWL	SCK Low Time	-	35	ns

\* The definition of signal timing is defined by SPI\_SCK=13.5MHz.

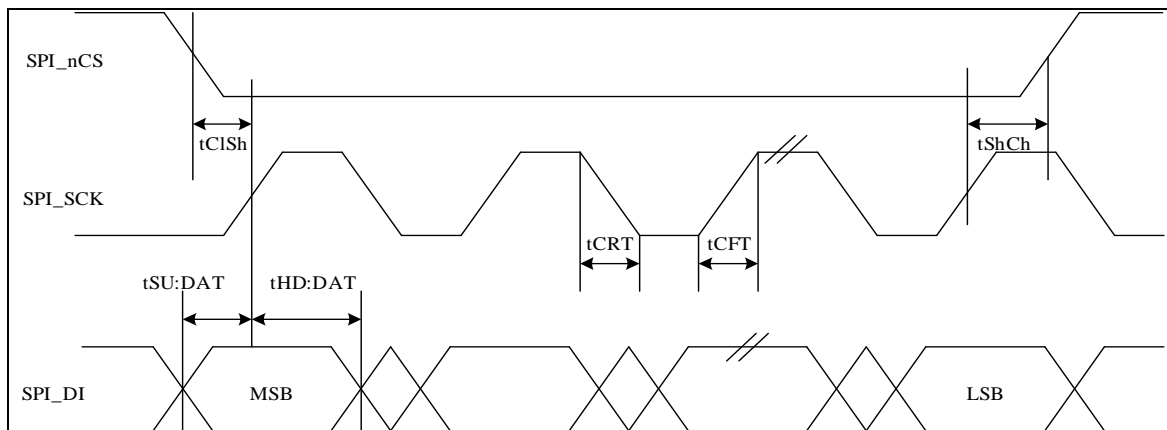


Figure 6.1: Input Timing Diagram of SPI

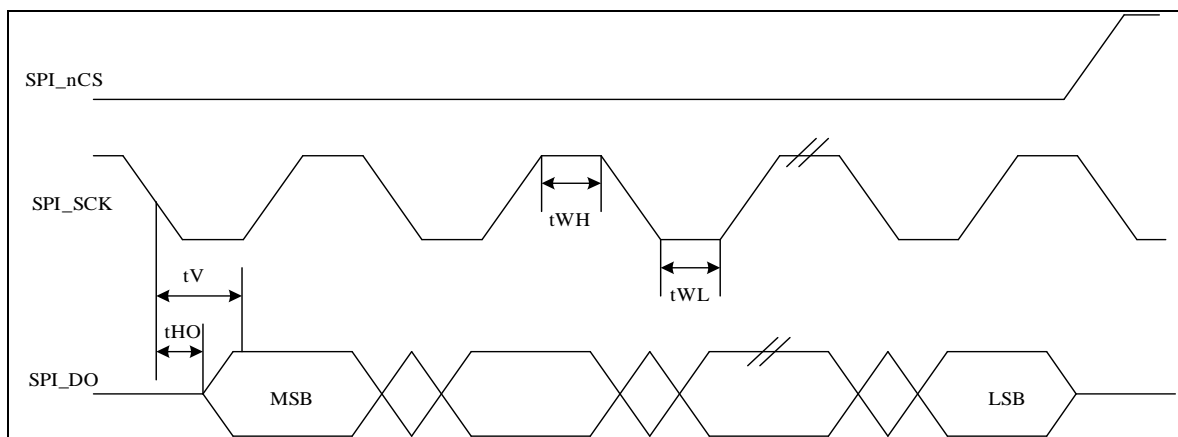


Figure 6.2: Output Timing Diagram of SPI

## 6.2 Inter-IC Sound Interface

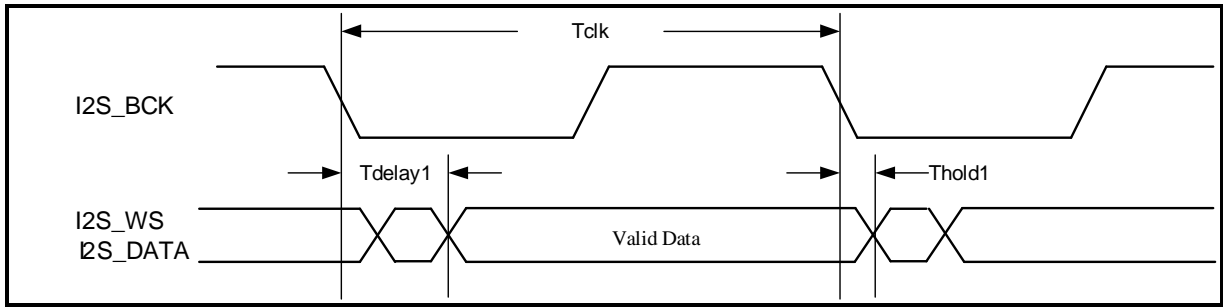


Figure 6.3: Timing Diagram of I2S

Symbol	Parameter	Min.	Max.	Unit
Tclk	Bit clock frequency	20.84	125	us
Tdelay1	output delay from CLK rising edge	0	3	ns
Thold1	output data hold time from CLK rising edge	0	3	ns

### 6.3 I2C Interface

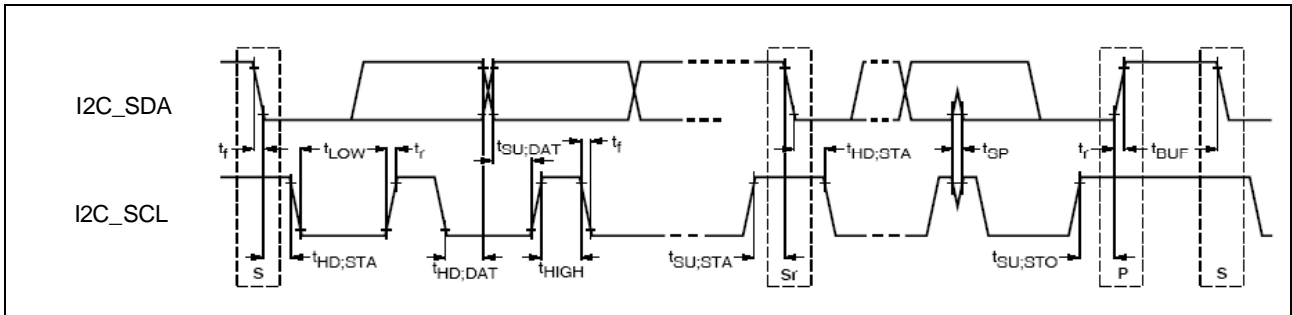


Figure 6.4: Timing Diagram of I2C-bus

Symbol	Parameter	Standard-Mode		Fast- Mode		Unit
		Min.	Max.	Min.	Max.	
$f_{SCL}$	SCL clock frequency	0	100	0	400	KHz
$t_{HD; STA}$	Hold time (repeated) START condition After this period, the first clock pulse is generated	4.0	-	0.6	-	us
$t_{LOW}$	LOW period of the SCL clock	4.7	-	1.3	-	us
$t_{HIGH}$	HIGH period of the SCL clock	4.0	-	0.6	-	us
$t_{SU; STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	us
$t_{HD; DAT}$	Data hold time for I2C bus devices	0	3.45	0	0.9	us
$t_{SU; DAT}$	Data set-up time	250	-	100	-	ns
$t_r$	Rise time of both SDA and SCL signals	-	1000	$20+0.1C_b$	300	ns
$t_f$	Fall time of both SDA and SCL signals	-	300	$20+0.1C_b$	300	ns
$t_{SU; DAT}$	Set-up time for STOP condition	4.0	-	0.6	-	us
$t_{BUF}$	Bus free time between a STOP and START condition	4.7	-	1.3	-	us
$C_b$	Capacitive load for each bus line	-	400	-	400	pF

Notes

1.  $C_b$  = total capacitance of one bus line in PF.
2. The maximum  $t_{HD;DAT}$  has only to be met if the device does not stretch the LOW period ( $t_{LOW}$ ) of the SCL signal.

### 6.4 SDRAM Interface

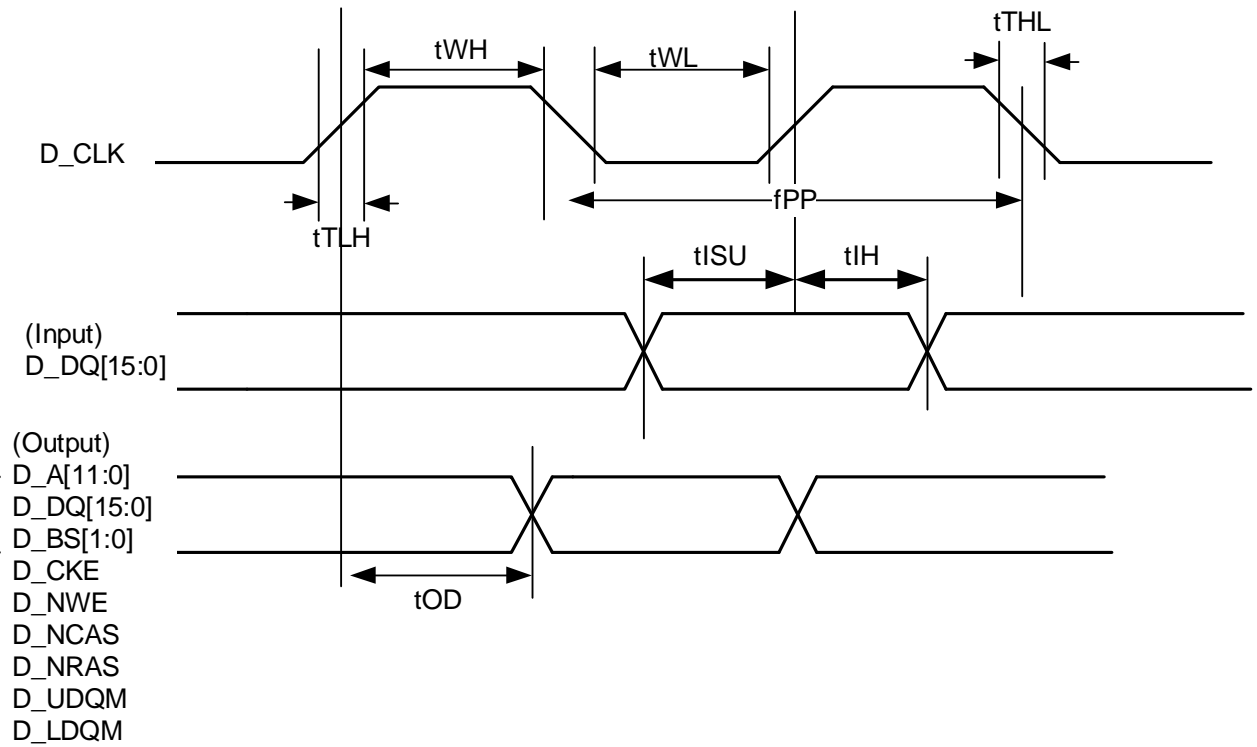


Figure 6.5: Timing Diagram of SDRAM Interface

Symbol	Parameter	Min.	Max.	Unit
fPP	Clock frequency	-	108	MHz
tWL	Clock low time	4.62	-	ns
tWH	Clock High time	4.62	-	ns
tTLH	Clock rise time		2	ns
tTHL	Clock fall time		2	ns
tISU	Input set-up time	2		ns
tIH	Input hold time	1		ns
tOD	Output delay time		3.5	ns

## 6.5 Secure Digital/ MultiMedia Card Interface

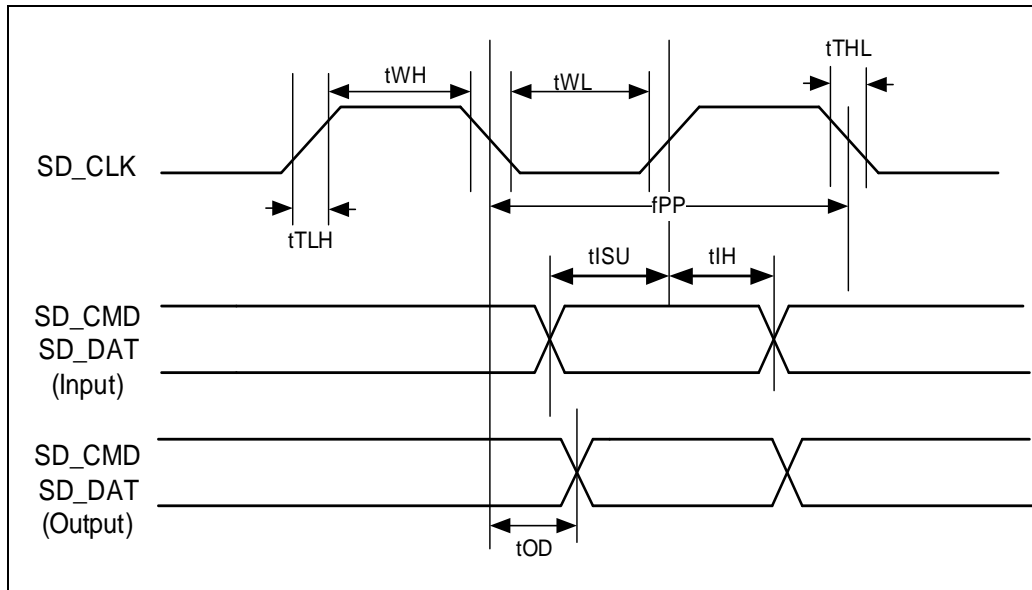


Figure 6.11: Timing Diagram of Data Input/Output Referenced to Clock

Symbol	Parameter	Min.	Max.	Unit
$f_{PP}$	Clock frequency	-	36	MHz
$t_{WL}$	Clock low time	20	-	ns
$t_{WH}$	Clock High time	7	-	ns
$t_{TLH}$	Clock rise time		3	ns
$t_{THL}$	Clock fall time		3	ns
$t_{ISU}$	Input setup time	10		ns
$t_{IH}$	Input hold time	5		ns
$t_{OD}$	Output delay time		3	ns

\* The definition of signal timing is defined by  $SD\_CLK=36MHz$ .



## 6.6 XD / NAND Flash Interface

Symbol	Parameter	Min.	Max.	Unit
tCLhWI	CLE high to $\overline{\text{WE}}$ low	27	-	ns
tWhCLI	$\overline{\text{WE}}$ high to CLE low	55	-	ns
tCIWI	$\overline{\text{CE}}$ low to $\overline{\text{WE}}$ low	27	-	ns
tWhCh	$\overline{\text{WE}}$ high to $\overline{\text{CE}}$ high	55	-	ns
tWP	$\overline{\text{WE}}$ pulse width	55	-	ns
tALhWI	ALE high to $\overline{\text{WE}}$ low	27	-	ns
tWhALI	$\overline{\text{WE}}$ high to ALE low	80	-	ns
tDS	Data setup time	10	-	ns
tDH	Data hold time	5	-	ns
tWC	Write cycle time	135	-	ns
tWH	$\overline{\text{WE}}$ high hold time	80	-	ns
tRR	Ready to $\overline{\text{RE}}$ Low	70	-	ns
tRP	Read pulse width	55	-	ns
tRC	Read cycle time	135	-	ns
tOD	$\overline{\text{WE}}$ output delay time	-	0	ns
tREH	$\overline{\text{RE}}$ high hold time	80	-	ns

- The definition of signal timing is defined by Peri\_clk=36MHz.
- The definition of read/write pulse width is defined with  $2*\text{Peri\_clk}$ , this timing can be redefined by setting register.
- The definition of read/write high hold time is defined with  $3*\text{Peri\_clk}$ , this timing can be redefined by setting register.

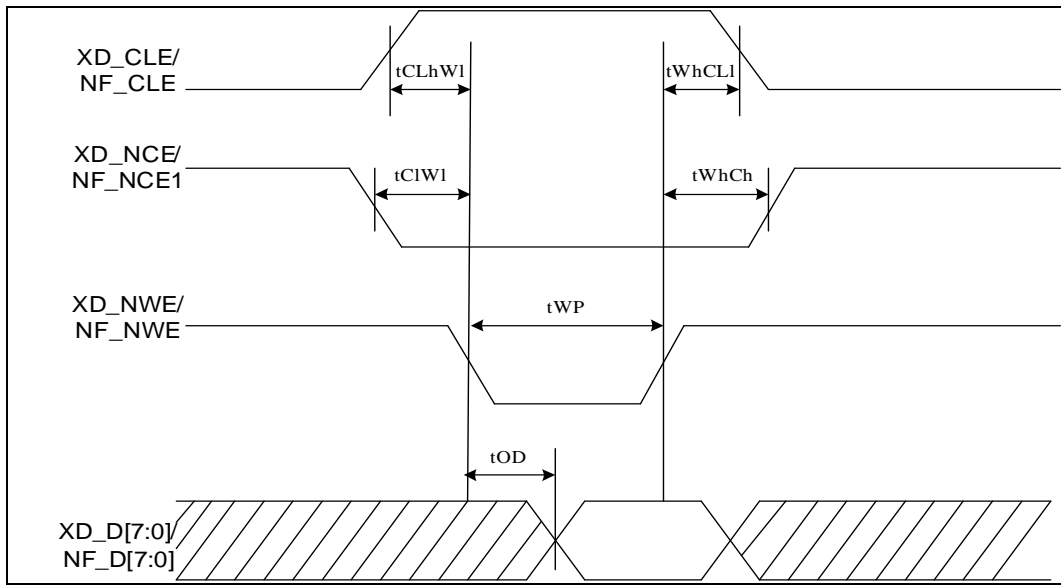


Figure 6.12: Command output Timing

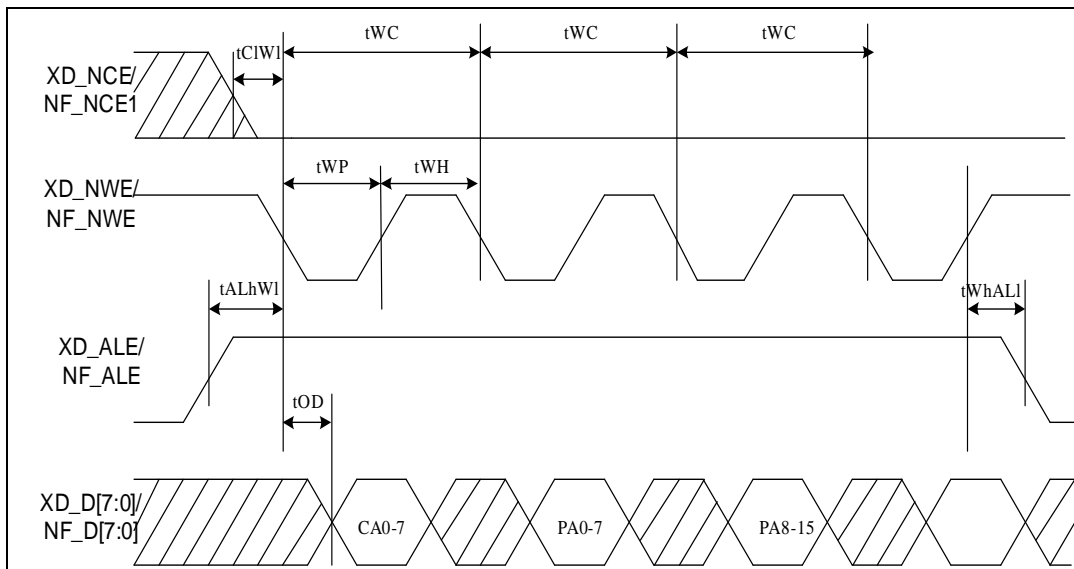


Figure 6.13: Address output Timing



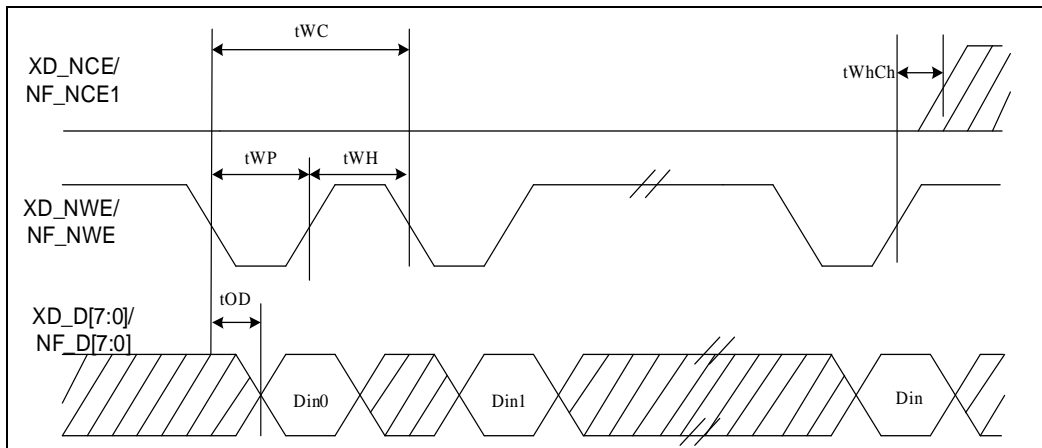


Figure 6.14: Data output Timing

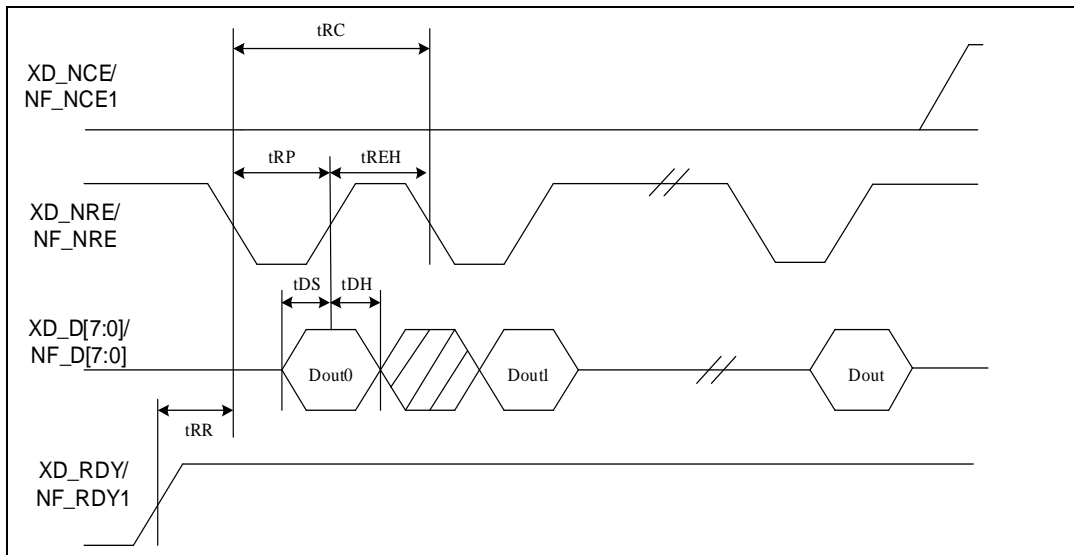


Figure 6.15: Data Input Timing



## 6.7 CompactFlash Card /ATA Interface

### ● True IDE PIO Mode Read/Write Timing Specification

Name	Item	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Note
t <sub>0</sub>	Cycle time(min)	600	383	240	180	120	100	80	
t <sub>1</sub>	Address Valid to CF_DIOR /CF_DIOW setup(min)	70	50	30	30	25	15	10	
t <sub>2</sub>	CF_DIOR/CF_DIOR (min)	165	125	100	80	70	65	55	
t <sub>2</sub>	CF_DIOR/CF_DIOR Register	290	290	290	80	70	65	55	
t <sub>2i</sub>	CF_DIOR/CF_DIOR Recovery time(min)	-	-	-	70	25	25	20	
t <sub>3</sub>	CF_DIOW data setup (min)	60	45	30	30	20	20	15	
t <sub>4</sub>	CF_DIOW data hold (min)	30	20	15	10	10	5	5	
t <sub>5</sub>	CF_DIOR data setup (min)	50	35	20	20	20	15	10	

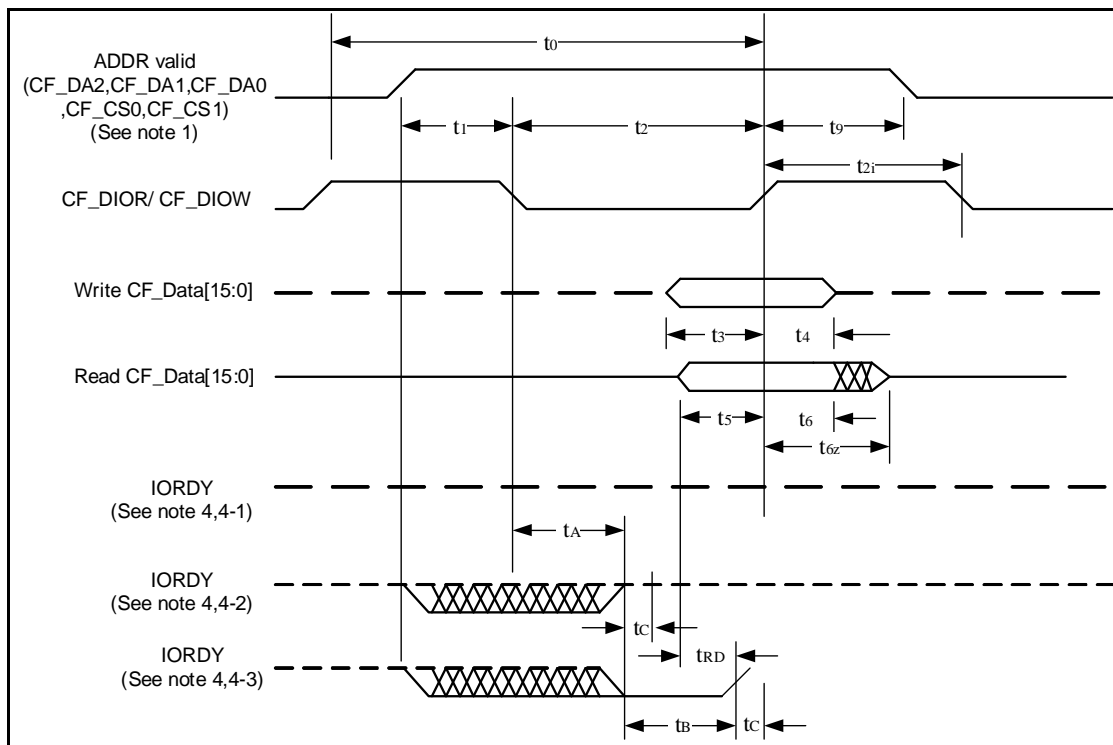


Figure 6.16: Timing Diagram of True IDE PIO Mode

Notes:

- (1) Device address consists of CF\_CS0, CF\_CS1, and CF\_DA [2:0]
- (2) Data consists of CF\_Data[15:00] (16-bit)
- (3) The negation of CF\_IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after  $t_A$  from the assertion of CF\_DIOR or CF\_DIOW. The assertion and negation of CF\_IORDY is described in the following three cases:
  - (4-1) Device never negates CF\_IORDY: No wait is generated.
  - (4-2) Device starts to drive CF\_IORDY low before  $t_A$ , but causes CF\_IORDY to be asserted before  $t_A$ : No wait generated.
  - (4-3) Device drives CF\_IORDY low before  $t_A$ : wait generated. The cycle completes after CF\_IORDY is reasserted. For cycles where a wait is generated and CF\_IORDY is asserted, the device shall place read data on CF\_Data[15:00] for  $t_{RD}$  before causing CF\_IORDY to be asserted.

● True IDE Multiword DMA Mode Read/Write Timing Specification

Name	Item	Mode0 (ns)	Mode1 (ns)	Mode2 (ns)	Mode3 (ns)	Mode4 (ns)
$t_o$	Cycle time(min)	480	150	120	100	80
$t_D$	CF_DIOR/CF_DIOW asserted width(min)	215	80	70	65	55
$t_E$	CF_DIOR data access(max)	150	60	50	50	45
$t_F$	CF_DIOR data hole(min)	5	5	5	5	5
$t_G$	CF_DIOR/CF_DIOW data setup(min)	100	30	20	15	10
$t_H$	CF_DIOW data hold(min)	20	15	10	5	5
$t_I$	CF_DMACK to CF_DIOR/CF_DIOW setup(min)	0	0	0	0	0
$t_J$	CF_DIOR/CF_DIOW to CF_DMACK hold(min)	20	5	5	5	5
$t_{KR}$	CF_DIOR negated width(min)	50	50	25	25	20
$t_{KW}$	CF_DIOW negated width(min)	215	50	25	25	20
$t_{LR}$	CF_DIOR to CF_DMARQ delay(max)	120	40	35	35	35
$t_{LW}$	CF_DIOW to CF_DMARQ delay(max)	40	40	35	35	35
$t_M$	CF_CS(1:0)valid to CF_DIOR/CF_DIOW	50	30	25	10	5
$t_N$	CF_CS(1:0) hold	15	10	10	10	10
$t_z$	CF_DMACK	20	25	25	25	25

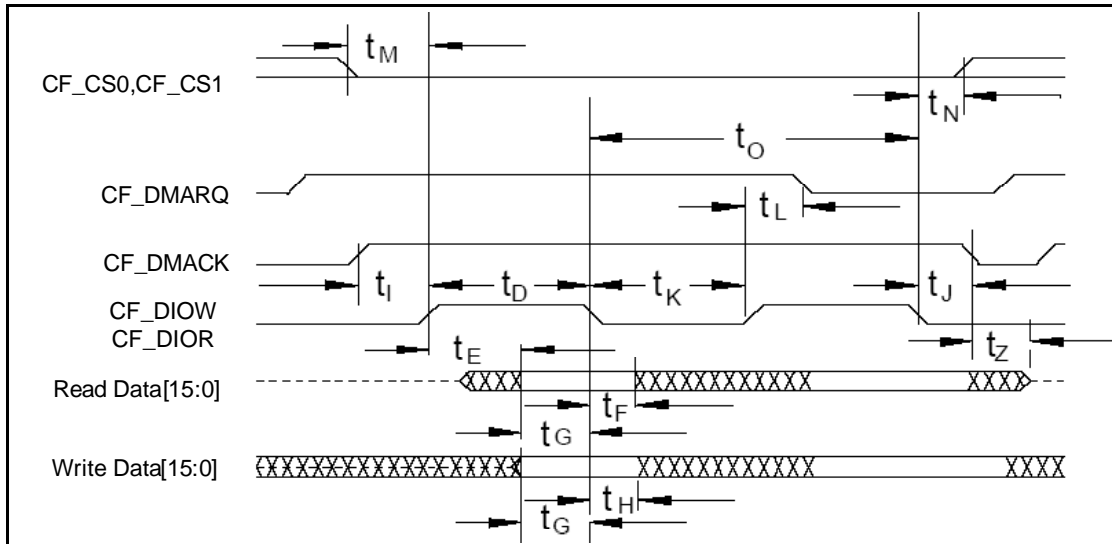


Figure 6.17: Timing Diagram of True IDE Multiword DMA Mode Read/Write



● True IDE Ultra DMA Mode Read/Write Timing Specification

Signal	Alias name for Ultra DMA Mode	Note
CF_DIOR	HDMARDY or HSTROBE	
CF_DIOW	STOP	
CF_IORDY	DDMARDY or DSTROBE	

Name	UDMA Mode0 (ns)		UDMA Mode1 (ns)		UDMA Mode2 (ns)		UDMA Mode3 (ns)		UDMA Mode4 (ns)		Measurement Location
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>2CYCTYP</sub>	240		160		120		90		60		Sender
t <sub>CYC</sub>	112		73		54		39		25		
t <sub>2CYC</sub>	230		153		115		86		57		Sender
t <sub>DS</sub>	15.0		10.0		7.0		7.0		5.0		Recipient
t <sub>DH</sub>	5.0		5.0		5.0		5.0		5.0		Recipient
t <sub>DVS</sub>	70.0		48.0		31.0		20.0		6.7		Sender
t <sub>DVH</sub>	6.2		6.2		6.2		6.2		6.2		Sender
t <sub>CS</sub>	15.0		10.0		7.0		7.0		5.0		Device
t <sub>CH</sub>	5.0		5.0		5.0		5.0		5.0		Device
t <sub>CVS</sub>	70.0		48.0		31.0		20.0		6.7		Host
t <sub>CVH</sub>	6.2		6.2		6.2		6.2		6.2		Host
t <sub>ZFS</sub>	0		0		0		0		0		Device
t <sub>DZFS</sub>	70.0		48.0		31.0		20.0		6.7		Sender
t <sub>FS</sub>		230		200		170		130		120	Device
t <sub>LI</sub>	0	150	0	150	0	150	0	100	0	100	
t <sub>MLI</sub>	20		20		20		20		20		Host
t <sub>UI</sub>	0		0		0		0		0		Host
t <sub>AZ</sub>		10		10		10		10		10	
t <sub>ZAH</sub>	20		20		20		20		20		Host
t <sub>ZAD</sub>	0		0		0		0		0		Device
t <sub>ENV</sub>	20	70	20	70	20	70	20	55	20	55	Host
t <sub>RFS</sub>		75		70		60		60		60	Sender
t <sub>RP</sub>	160		125		100		100		100		Recipient
t <sub>IORDYZ</sub>		20		20		20		20		20	Device
t <sub>ZIORDY</sub>	0		0		0		0		0		Device



$t_{ACK}$	20		20		20		20		20		Host
$t_{SS}$	50		50		50		50		50		Sender

Name	Comment	Note
$t_{2CYTYP}$	Typical sustained average two cycle time	
$t_{CYC}$	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
$t_{2CYC}$	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
$t_{DS}$	Data setup time at recipient (from data valid until STROBE edge)	
$t_{DH}$	Data hold time at recipient (from STROBE edge until data may become invalid)	
$t_{DVS}$	Data valid setup time at sender (from data valid until STROBE edge)	
$t_{DVH}$	Data valid hold time at sender (from STROBE edge until data may become invalid)	
$t_{CS}$	CRC word setup time at device	
$t_{CH}$	CRC word hold time device	
$t_{CVS}$	CRC word valid setup time at host (from CRC valid until -DMACK negation)	
$t_{CVH}$	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	
$t_{ZFS}$	Time from STROBE output released-to-driving until the first transition of critical timing.	
$t_{DZFS}$	Time from data output released-to-driving until the first transition of critical timing.	
$t_{FS}$	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
$t_{LI}$	Limited interlock time	
$t_{MLI}$	Interlock time with minimum	
$t_{UI}$	Unlimited interlock time	
$t_{AZ}$	Maximum time allowed for output drivers to release (from asserted or negated)	
$t_{ZAH}$	Minimum delay time required for output	
$t_{ZAD}$	Drivers to assert or negate (from released)	
$t_{ENV}$	Envelope time (from -DMACK so STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
$t_{RFS}$	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
$t_{RP}$	Ready-to-pause time (that recipient shall wait to pause after	

Name	Comment	Note
$t_{2CYTYP}$	Typical sustained average two cycle time	
$t_{CYC}$	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
$t_{2CYC}$	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
$t_{DS}$	Data setup time at recipient (from data valid until STROBE edge negating $\text{-DMARDY}$ )	
$t_{IORDYZ}$	Maximum time before releasing IORDY	
$t_{ZIORDY}$	Minimum time before driving IORDY	
$t_{ACK}$	Setup and hold times for $\text{-DMACK}$ (before assertion or negation)	
$t_{SS}$	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

● Initial an Ultra DMA Data-In Burst

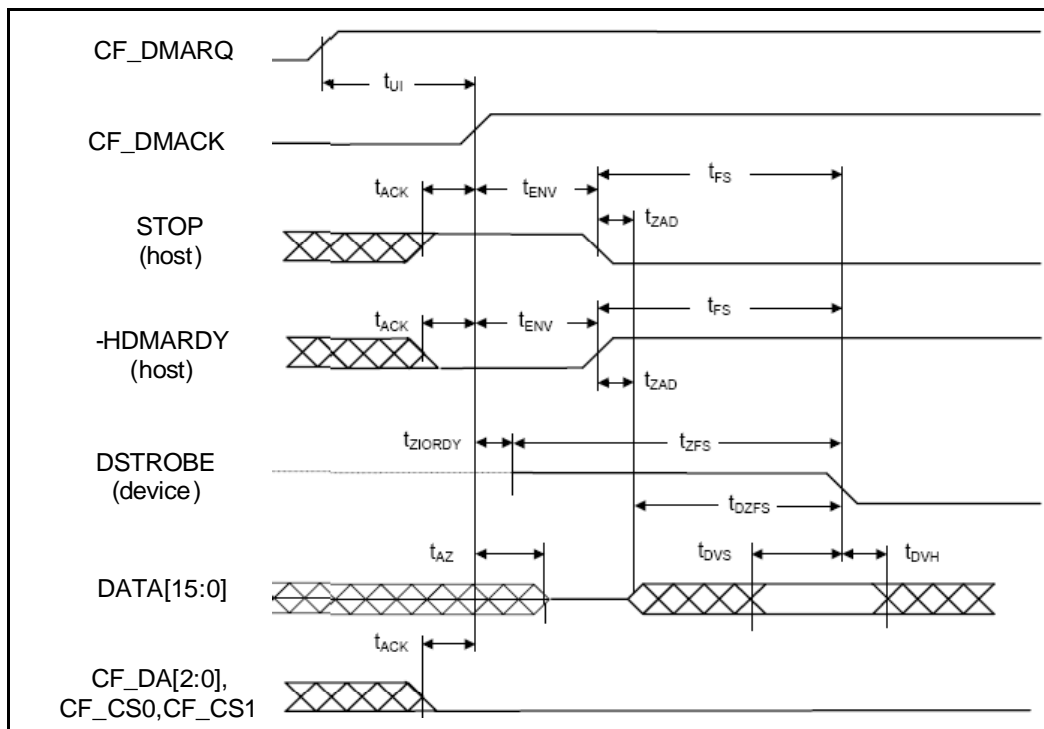


Figure 6.18: Initiation Timing Diagram of Ultra DMA Data-In Burst

● Sustaining an Ultra DMA Data-In Burst

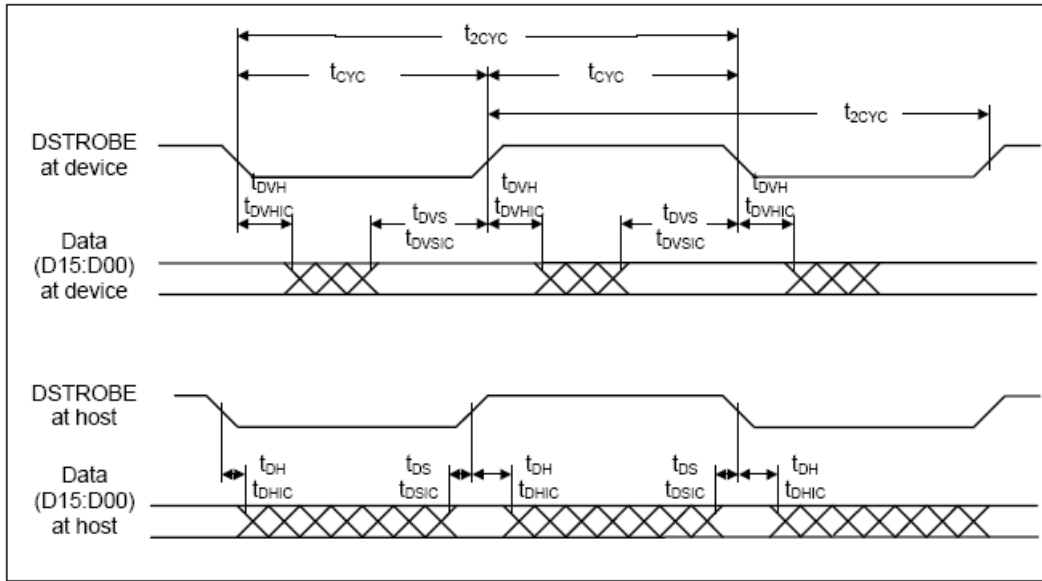
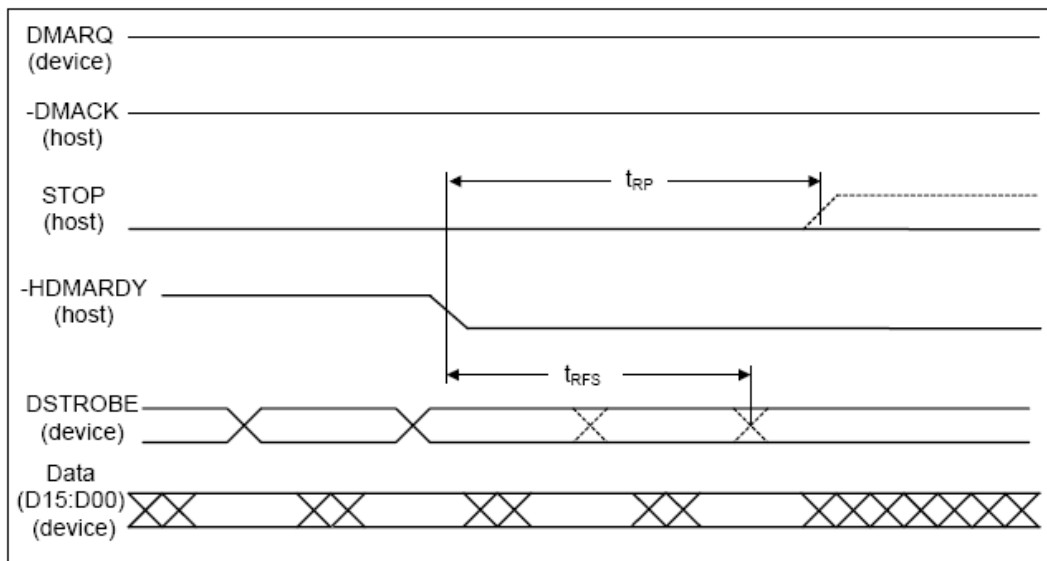


Figure 6.19: Sustained Ultra DMA Data-In Burst Timing Diagram

● Host Pausing an Ultra DMA Data-In Burst



Notes: 1) The host may assert STOP to request termination of the Ultra DMA burst no sooner than  $t_{RP}$  after  $\text{-HDMARDY}$  is negated.

2) After negating  $\text{-HDMARDY}$ , the host may receive zero, one, two, or three more data words from the device.

Figure 6.20: Ultra DMA Data-In Burst Host Pause Timing Diagram



● Device Terminating an Ultra Data-In Burst

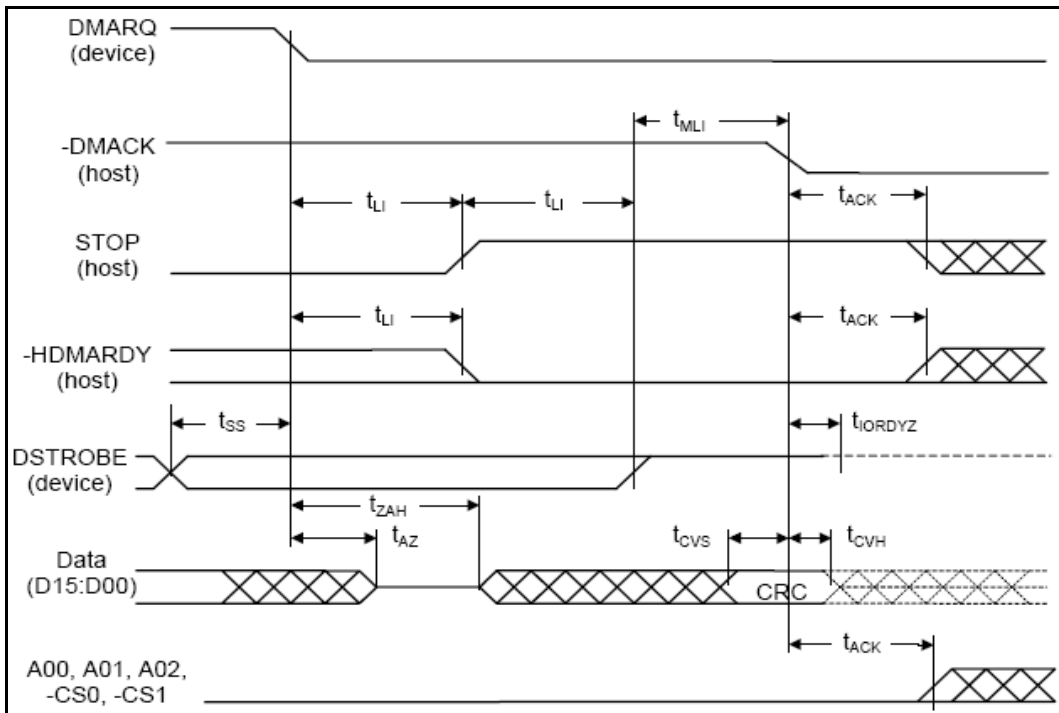


Figure 6.21: Ultra DMA Data-In Burst Device Termination Timing Diagram

● Host Terminating an Ultra DMA Data-In Burst

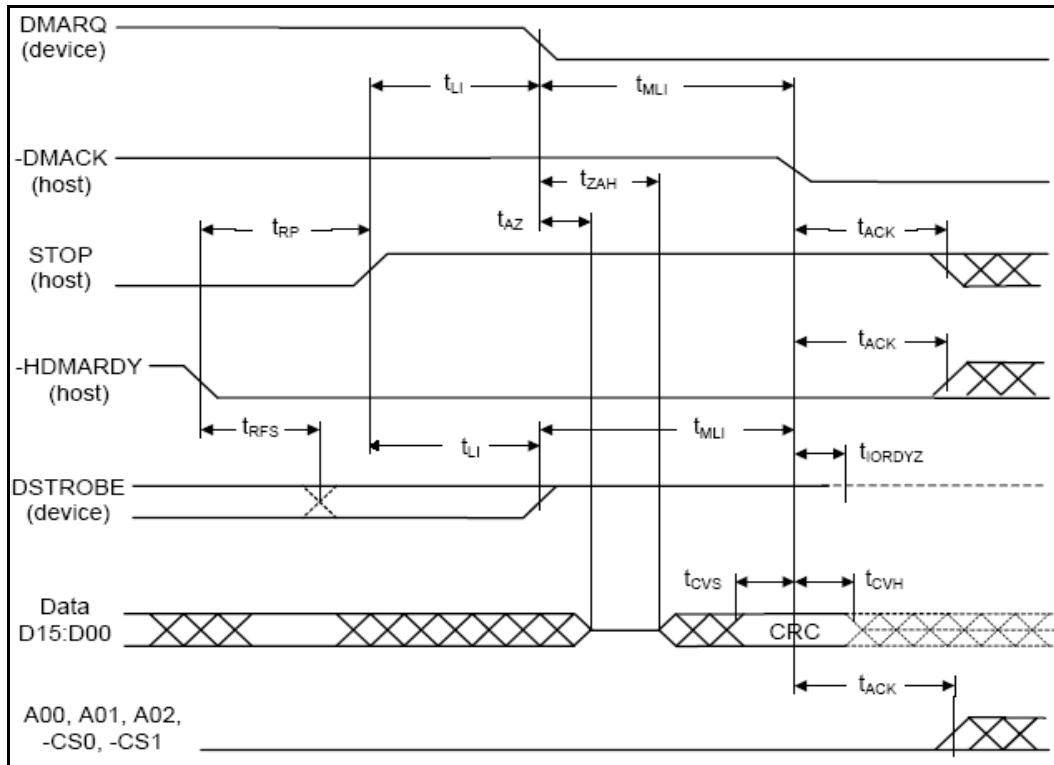


Figure 6.22: Ultra DMA Data-In Burst Host Termination Timing Diagram

- Initial an Ultra DMA Data-Out Burst

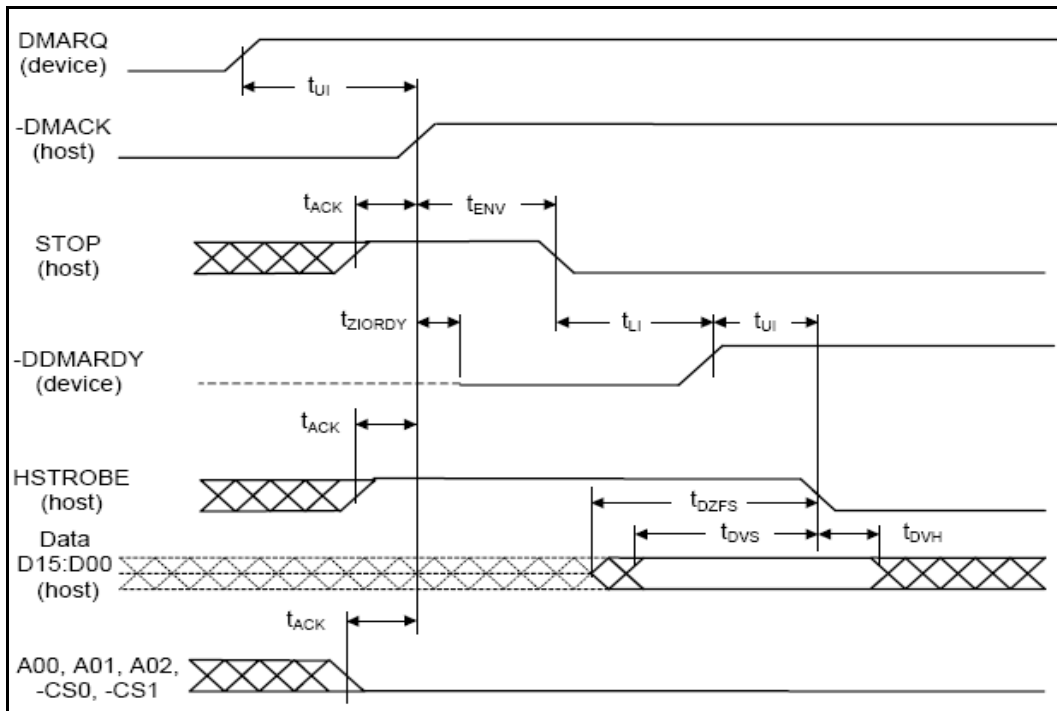


Figure 6.23: Ultra DMA Data-Out Burst Initiation Timing Diagram

- Sustaining an Ultra DMA Data-out Burst

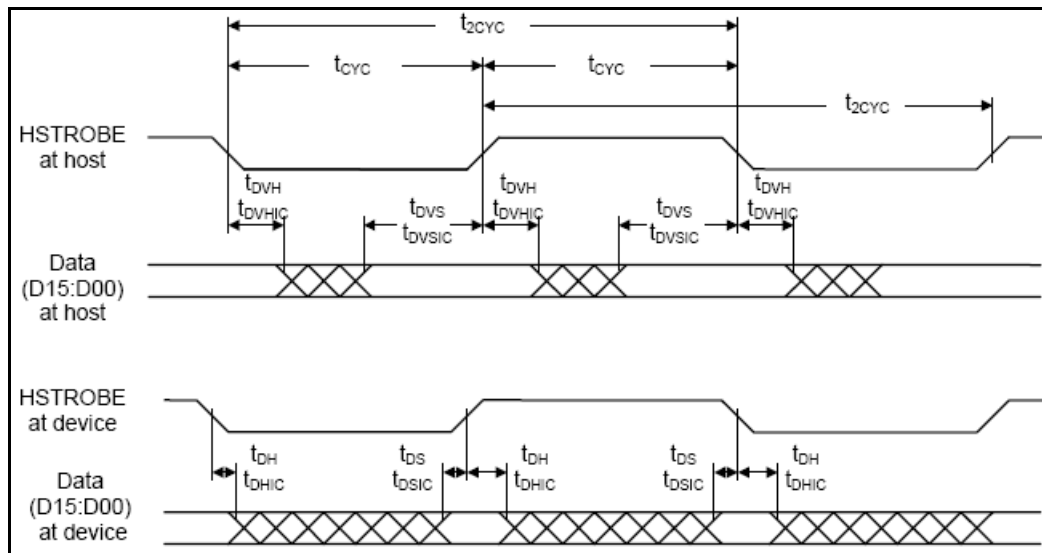


Figure 6.24: Sustained Ultra DMA Data-Out Burst Timing Diagram

● **Device Pausing an Ultra DMA Data-Out Burst**

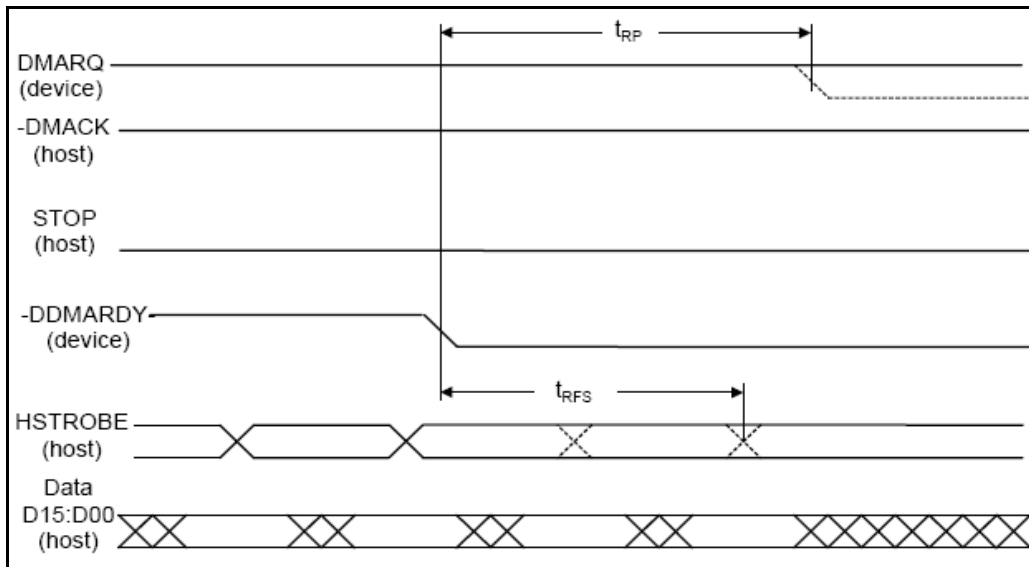


Figure 6.25: Ultra DMA Data-Out Burst Device Pause Timing Diagram

● **Device Terminating an Ultra DMA Data-Out Burst**

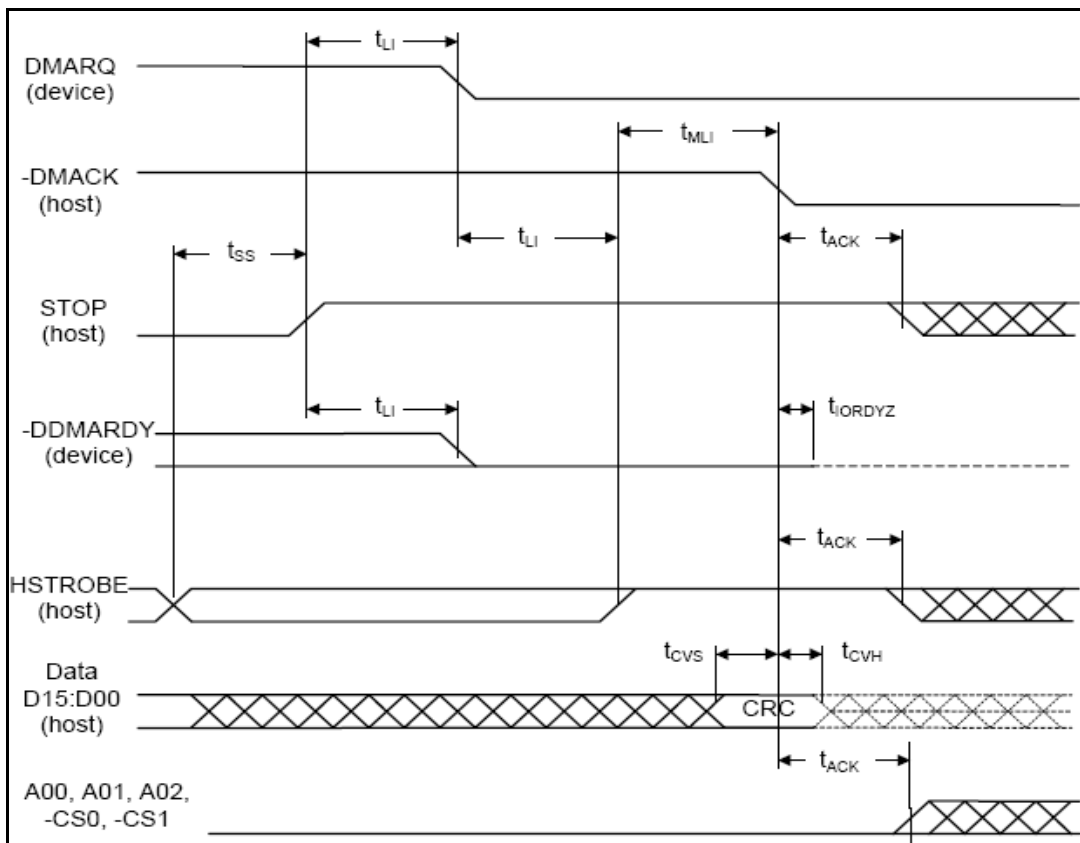


Figure 6.26: Ultra DMA Data-Out Burst Device Termination Timing Diagram

### 6.8 Digital Display Interface

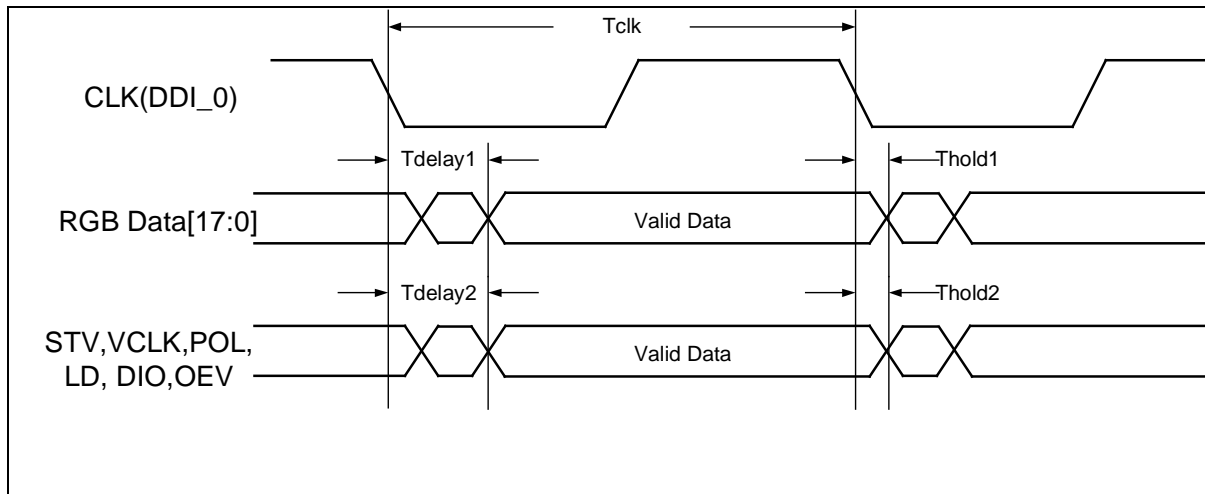


Figure 6.27: Timing Diagram of Digital Display Interface

Symbol	Parameter	Min.	Max.	Unit
Fclk	Pixel clock frequency (Fclk = 1/Tclk)	25	32	MHz
Tdelay1	RGB Data output delay from CLK rising edge	0	5	ns
Thold1	RGB Data output data hold time from CLK rising edge	0	5	ns
Tdelay2	STV, VCLK, POL, LD, DIO, OEV output delay from CLK rising edge	0	3	ns
Thold2	STV, VCLK, POL, LD, DIO, OEV output data hold time from CLK rising edge	0	3	ns



7. Electrical Characteristic

- Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V <sub>CC</sub>	Power Supply (3.3V)	-0.3 to 3.6	V
V <sub>CC1</sub>	Power Supply (1.8V)	-0.3 to 1.98	V
V <sub>IN</sub>	Input Voltage	-0.3 to V <sub>CC</sub> +0.3	V
V <sub>OUT</sub>	Output Voltage	-0.3 to V <sub>CC</sub> +0.3	V
T <sub>STG</sub>	Storage Temperature	-55 to 150	°C

- Recommended Operation Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V <sub>CC</sub>	Power Supply (3.3V)	3.0	3.3	3.6	V
V <sub>CC1</sub>	Power Supply (1.8V)	1.62	1.8	1.98	V
T <sub>OPR</sub>	Operating Temperature	0	25	70	°C

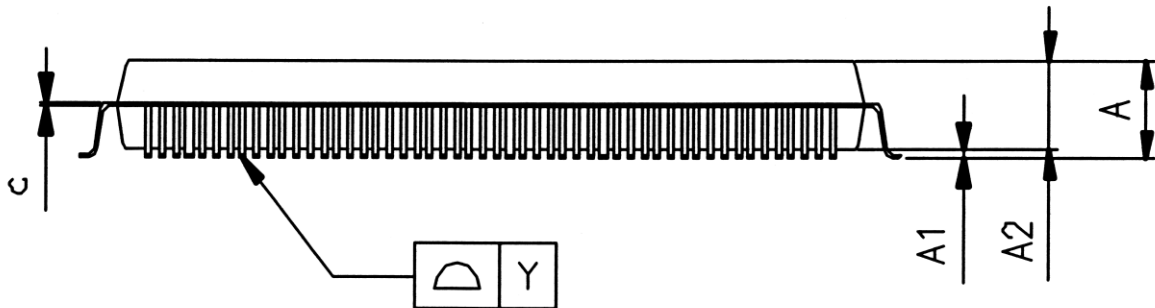
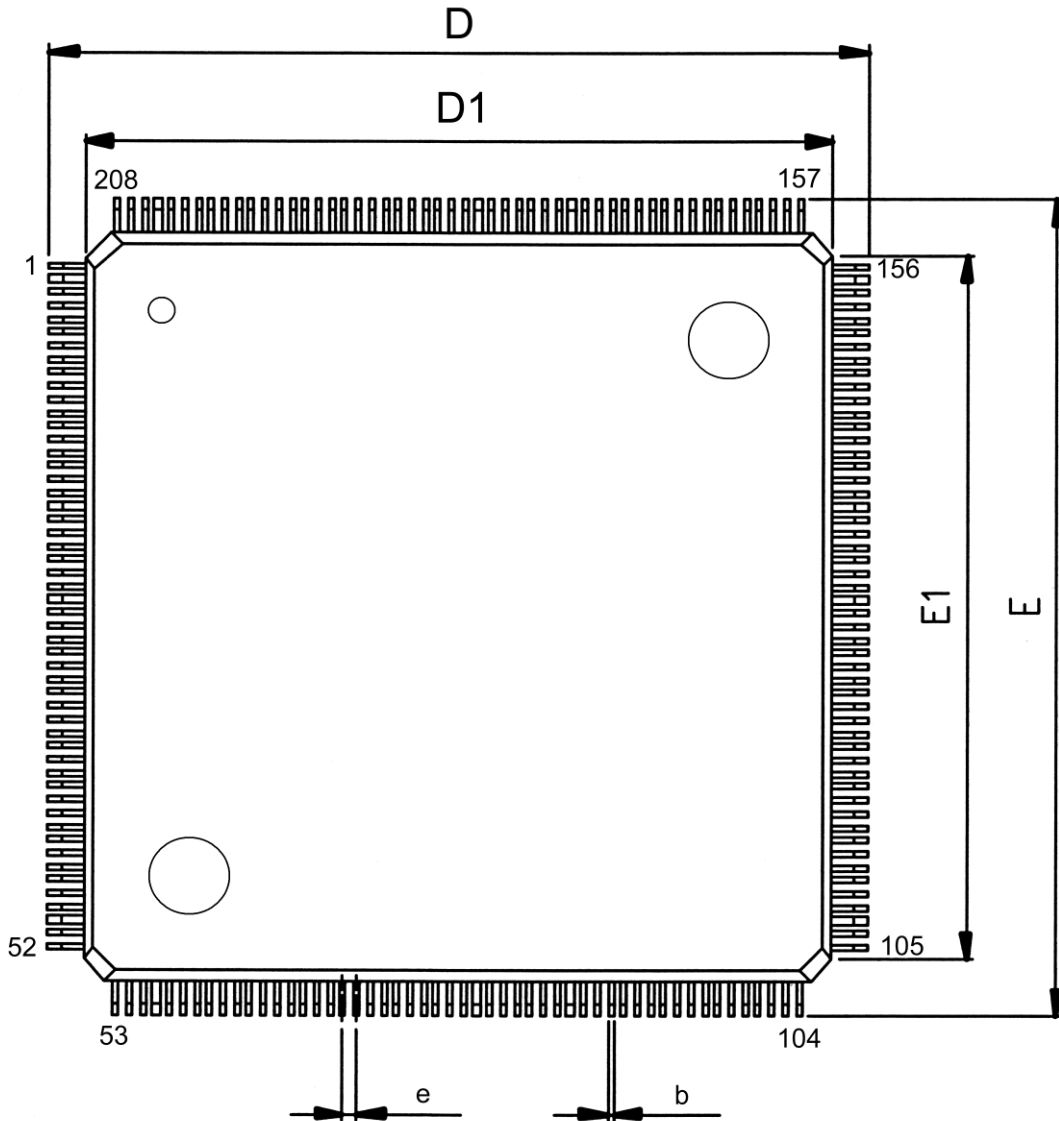
- DC Electrical Characteristics for 3.3 volts operation

(Under Recommended Operating Conditions and V<sub>CC</sub> = 3.0V ~ 3.6V, T<sub>j</sub> = 0°C to + 70°C)

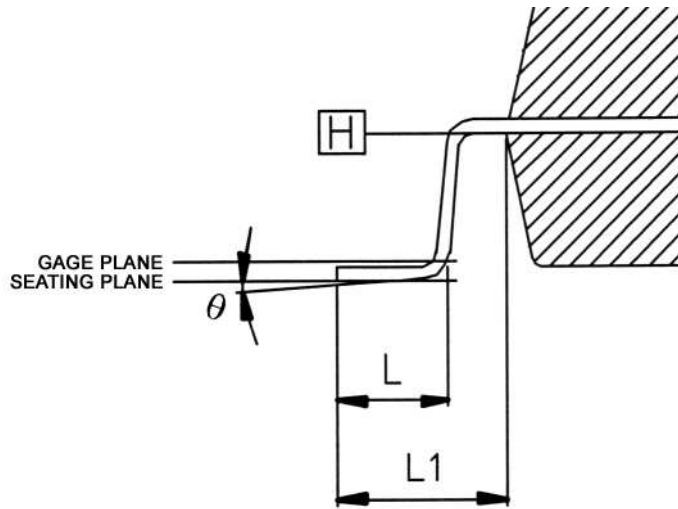
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V <sub>IL</sub>	Input Low Voltage		-0.3		0.8	V
V <sub>IL</sub>	Input Low Voltage		-0.3		0.8	V
V <sub>IH</sub>	Input High Voltage		2.0		V <sub>CC</sub> +0.3	V
V <sub>T-</sub>	Schmitt Input Low Voltage		-0.3		0.8	V
V <sub>T+</sub>	Schmitt Input High Voltage		2.0		V <sub>CC</sub> +0.3	V
V <sub>OL</sub>	Output Low Voltage				0.4	V
V <sub>OH</sub>	Output High Voltage		2.4			V

## 8. Package Outline and Dimension

- Package Outline (208-pin PQFP)



- Package Outline (208-pin PQFP) – continued



- Dimension (208-pin PQFP)

Dimension	Min	Nom	Max
A	-	-	4.10
A1	0.25	-	0.50
A2	3.20	3.40	3.60
b	0.17	-	0.27
c	0.11	-	0.23
D	31.20 BSC		
D1	28.00 BSC		
E	31.20 BSC		
E1	28.00 BSC		
e	0.50 BSC		
L	0.73	0.88	1.03
L1	1.60 REF		
Y	-	-	0.08
θ	0°	-	8°

Unit: mm

REF: Reference

BSC: Basic Spacing between Centers (integrated circuit package dimension)



## 9. Chip Revision History

Revision	Description of Changes	Date
JL4203A	First Announce	2007/3/20
JL4203A-V2	<ul style="list-style-type: none"><li>• Correct core voltage to 1.8 volts.</li><li>• Fix some bugs in MP3 block.</li><li>• Modify the function of internal pattern generator to control backlight brightness of LCD panel via GPIO_33 (pin 90).</li></ul>	2008/2/15

## 10. Ordering Information

Part Number	Package	Status	Note
JL4203A-V2	208-pin PQFP	Available	N/C





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