12-Bit, 1-MSPS, MICRO-POWER, MINIATURE SAR ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **1-MHz Sample Rate Serial Device**
- **12-Bit Resolution**
- **Zero Latency**
- **20-MHz Serial Interface**
- **Supply Range: 2.35 V to 5.25 V**
- **Typical Power Dissipation at 1 MSPS:**
  - **– 3.9 mW at 3-V V_{DD}**
  - **– 7.5 mW at 5-V V_{DD}**
- **INL ±1.25 LSB Maximum, ±0.65 LSB (Typical)**
- **DNL ±1 LSB Maximum, +0.4 / -0.65 LSB (Typical)**
- **Typical AC Performance: 72.25 dB SINAD, -84 dB THD**
- **Unipolar Input Range: 0 V to V_{DD}**
- **Power Down Current: 1 µA**
- **Wide Input Bandwidth: 15 MHz at 3 dB**
- **6-Pin SOT23 and SC70 Packages**

APPLICATIONS

- **Base Band Converters in Radio Communication**
- **Motor Current/Bus Voltage Sensors in Digital Drives**
- **Optical Networking (DWDM, MEMS Based Switching)**
- **Optical Sensors**
- **Battery Powered Systems**
- **Medical Instrumentations**
- **High-Speed Data Acquisition Systems**
- **High-Speed Closed-Loop Systems**

DESCRIPTION

The ADS7886 is a 12-bit, 1-MSPS analog-to-digital converter (ADC). The device includes a capacitor based SAR A/D converter with inherent sample and hold. The serial interface in each device is controlled by the $\overline{CS}$ and SCLK signals for glueless connections with microprocessors and DSPs. The input signal is sampled with the falling edge of $\overline{CS}$, and SCLK is used for conversion and serial data output.

The device operates from a wide supply range from 2.35 V to 5.25 V. The low power consumption of the device makes it suitable for battery-powered applications. The device also includes a powerdown feature for power saving at lower conversion speeds.

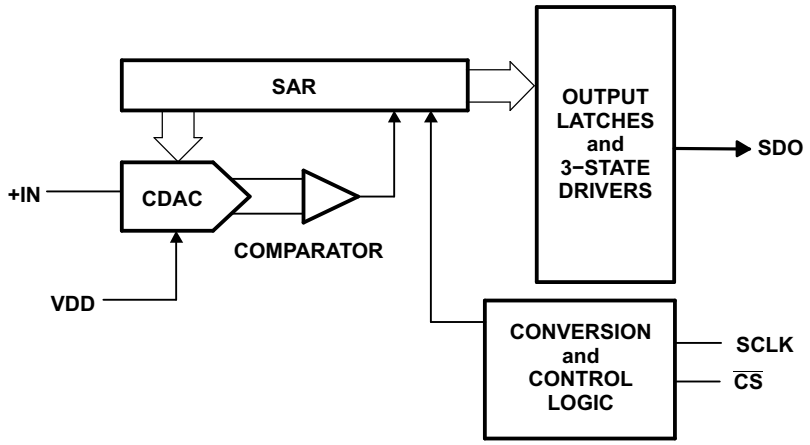
The high level of the digital input to the device is not limited to device V_{DD}. This means the digital input can go as high as 5.25 V when device supply is 2.35 V. This feature is useful when digital signals are coming from other circuit with different supply levels. Also this relaxes restriction on power up sequencing.

The ADS7886 is available in 6-pin SOT23 and SC70 packages and is specified for operation from -40°C to 125°C.

Micro-Power Miniature SAR Converter Family

BIT	< 300 KSPS	300 KSPS – 1.25 MSPS
12-Bit	ADS7866 (1.2 V_{DD} to 3.6 V_{DD})	ADS7886 (2.35 V_{DD} to 5.25 V_{DD})
10-Bit	ADS7867 (1.2 V_{DD} to 3.6 V_{DD})	ADS7887 (2.35 V_{DD} to 5.25 V_{DD})
8-Bit	ADS7868 (1.2 V_{DD} to 3.6 V_{DD})	ADS7888 (2.35 V_{DD} to 5.25 V_{DD})

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



PACKAGE/ORDERING INFORMATION(1)

DEVICE	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	PACKAGE MARKING	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
ADS7886SB	±1.25	±1	12	6-Pin SOT23	DBV	–40°C to 125°C	BBAQ	ADS7886SBDBVT	Tape and reel 250
								ADS7886SBDBVR	Tape and reel 3000
				6-Pin SC70	DCK		BNL	ADS7886SBDCKT	Tape and reel 250
								ADS7886SBDCKR	Tape and reel 3000
ADS7886S	±2	±2	11	6-Pin SOT23	DBV	–40°C to 125°C	BBAQ	ADS7886SDBVT	Tape and reel 250
								ADS7886SDBVR	Tape and reel 3000
				6-Pin SC70	DCK		BNL	ADS7886SDCKT	Tape and reel 250
								ADS7886SDCKR	Tape and reel 3000

(1) For most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		UNIT
+IN to AGND		–0.3 V to +V_{DD} +0.3 V
+V_{DD} to AGND		–0.3 V to 7 V
Digital input voltage to GND		–0.3 V to (7 V)
Digital output to GND		–0.3 V to (+V_{DD} + 0.3 V)
Operating temperature range		–40°C to 125°C
Storage temperature range		–65°C to 150°C
Junction temperature (T_J Max)		150°C
Power dissipation, SOT23 and SC70 packages		(T_J Max–T_A)/θ_{JA}
θ_{JA} Thermal impedance	SOT23	295.2°C/W
	SC70	351.3°C/W
Lead temperature, soldering	Vapor phase (60 sec)	215°C
	Infrared (15 sec)	220°C

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

+V_{DD} = 2.35 V to 5.25 V, T_A = –40°C to 125°C, $f_{(sample)}$ = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input voltage span(1)		0		V_{DD}	V
	Absolute input voltage range	+IN	–0.2		V_{DD}+0.2	V
C_I	Input capacitance(2)			21		pF
I_{lkg}	Input leakage current	T_A = 125°C		40		nA
SYSTEM PERFORMANCE						
	Resolution			12		Bits
	No missing codes	ADS7886SB	12			Bits
		ADS7886S	11			
INL	Integral nonlinearity	ADS7886SB	–1.25	±0.65	1.25	LSB(3)
		ADS7886S	2		2	
DNL	Differential nonlinearity	ADS7886SB	–1	+0.4/-0.65	1	LSB
		ADS7886S	-2		2	
E_O	Offset error(4)	V_{DD} = 2.35 V to 3.6 V	–2.5	±0.5	2.5	LSB
		V_{DD} = 4.75 V to 5.25 V	-2	±0.5	2	
E_G	Gain error		–1.75	±0.5	1.75	LSB
SAMPLING DYNAMICS						
	Conversion time	20-MHz SCLK	760	800		ns
	Acquisition time		325			ns
	Maximum throughput rate	20-MHz SCLK			1	MHz
	Aperture delay			5		ns
	Step Response			160		ns
	Overvoltage recovery			160		ns
DYNAMIC CHARACTERISTICS						
SNR	Signal-to-noise ratio	V_{DD} = 2.35 V to 3.6 V, f_I = 100 kHz	69	71.25		dB
		V_{DD} = 4.75 V to 5.25 V, f_I = 100 kHz	70	72.25		

(1) Ideal input span; does not include gain or offset error.
(2) See Figure 28 for details on the sampling circuit.
(3) LSB means least significant bit.
(4) Measured relative to an ideal full-scale input.

ELECTRICAL CHARACTERISTICS (continued)

+V_{DD} = 2.35 V to 5.25 V, T_A = –40°C to 125°C, $f_{(sample)}$ = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise and distortion	V_{DD} = 2.35 V to 3.6 V, f_I = 100 kHz	69	71.25		dB
		V_{DD} = 4.75 V to 5.25 V, f_I = 100 kHz	70	72.25		
THD	Total harmonic distortion(5)	f_I = 100 kHz		–84		dB
SFDR	Spurious free dynamic range	f_I = 100 kHz		85.5		dB
	Full power bandwidth	At –3 dB		15		MHz
DIGITAL INPUT/OUTPUT						
Logic family — CMOS						
V_{IH}	High-level input voltage	V_{DD} = 2.35 V to 5.25 V	V_{DD}– 0.4		5.25	V
V_{IL}	Low-level input voltage	V_{DD} = 5 V			0.8	V
		V_{DD} = 3 V			0.4	
V_{OH}	High-level output voltage	$I_{(source)}$ = 200 µA	V_{DD}–0.2			V
V_{OL}	Low-level output voltage	$I_{(sink)}$ = 200 µA			0.4	
POWER SUPPLY REQUIREMENTS						
+V_{DD}	Supply voltage		2.35	3.3	5.25	V
	Supply current (normal mode)	V_{DD} = 2.35 V to 3.6 V, 1-MHz throughput		1.3	1.5	mA
		V_{DD} = 4.75 V to 5.25 V, 1-MHz throughput		1.5	2	
		V_{DD} = 2.35 V to 3.6 V, static state			1.1	
		V_{DD} = 4.75 V to 5.25 V, static state			1.5	
	Power down state supply current	SCLK off			1	µA
		SCLK on (20 MHz)			200	
	Power dissipation at 1-MHz throughput	V_{DD} = 3 V		3.9	4.5	mW
		V_{DD} = 5 V		7.5	10	
	Power dissipation in static state	V_{DD} = 3 V			3.3	mW
		V_{DD} = 5 V			7.5	
	Power up time				0.1	µs
	Invalid conversions after power up or reset				1	

(5) Calculated on the first nine harmonics of the input frequency.

TIMING REQUIREMENTS (see Figure 1 and Figure 2)

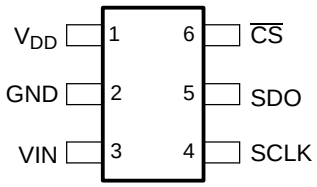
All specifications typical at T_A = –40°C to 125°C, V_{DD} = 2.35 V to 5.25 V (unless otherwise specified).

PARAMETER			TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
t_{conv}	Conversion time	ADS7866	V_{DD} = 3 V			16 × t_{SCLK}	ns
			V_{DD} = 5 V			16 × t_{SCLK}	
t_q	Minimum quiet time needed from bus 3-state to start of next conversion		V_{DD} = 3 V	40			ns
			V_{DD} = 5 V	40			
t_{d1}	Delay time, $\overline{CS}$ low to first data (0) out		V_{DD} = 3 V		15	25	ns
			V_{DD} = 5 V		13	25	
t_{su1}	Setup time, $\overline{CS}$ low to SCLK low		V_{DD} = 3 V	10			ns
			V_{DD} = 5 V	10			
t_{d2}	Delay time, SCLK falling to SDO		V_{DD} = 3 V		15	25	ns
			V_{DD} = 5 V		13	25	
t_{h1}	Hold time, SCLK falling to data valid(2)		V_{DD} < 3 V	7			ns
			V_{DD} > 5 V	5.5			
t_{d3}	Delay time, 16th SCLK falling edge to SDO 3-state		V_{DD} = 3 V		10	25	ns
			V_{DD} = 5 V		8	20	
t_{w1}	Pulse duration, $\overline{CS}$		V_{DD} = 3 V	25	40		ns
			V_{DD} = 5 V	25	40		
t_{d4}	Delay time, $\overline{CS}$ high to SDO 3-state		V_{DD} = 3 V		17	30	ns
			V_{DD} = 5 V		15	25	
t_{wH}	Pulse duration, SCLK high		V_{DD} = 3 V	0.4 × t_{SCLK}			ns
			V_{DD} = 5 V	0.4 × t_{SCLK}			
t_{wL}	Pulse duration, SCLK low		V_{DD} = 3 V	0.4 × t_{SCLK}			ns
			V_{DD} = 5 V	0.4 × t_{SCLK}			
	Frequency, SCLK		V_{DD} = 3 V			20	MHz
			V_{DD} = 5 V			20	
t_{d5}	Delay time, second falling edge of clock and $\overline{CS}$ to enter in powerdown (use min spec not to accidently enter in powerdown) Figure 2		V_{DD} = 3 V	-2		5	ns
			V_{DD} = 5 V	-2		5	
t_{d6}	Delay time, $\overline{CS}$ and 10th falling edge of clock to enter in powerdown (use max spec not to accidently enter in powerdown) Figure 2		V_{DD} = 3 V	2		-5	ns
			V_{DD} = 5 V	2		-5	

(1) 3-V Specifications apply from 2.35 V to 3.6 V, and 5-V specifications apply from 4.75 V to 5.25 V.
(2) With 50-pf load.

DEVICE INFORMATION

SOT23/SC70 PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
V_{DD}	1	–	Power supply input also acts like a reference voltage to ADC.
GND	2	–	Ground for power supply, all analog and digital signals are referred with respect to this pin.
VIN	3	I	Analog signal input
SCLK	4	I	Serial clock
SDO	5	O	Serial data out
$\overline{CS}$	6	I	Chip select signal, active low

NORMAL OPERATION

The cycle begins with the falling edge of $\overline{CS}$. This point is indicated as **a** in Figure 1. With the falling edge of $\overline{CS}$, the input signal is sampled and the conversion process is initiated. The device outputs data while the conversion is in progress. The data word contains 4 leading zeros, followed by 12-bit data in MSB first format.

The falling edge of $\overline{CS}$ clocks out the first zero, and a zero is clocked out on every falling edge of the clock until the third edge. Data is in MSB first format with the MSB being clocked out on the 4th falling edge. On the 16th falling edge of SCLK, SDO goes to the 3-state condition. The conversion ends on the 16th falling edge of SCLK. The device enters the acquisition phase on the first rising edge of SCLK after the 13th falling edge. This point is indicated by **b** in Figure 1.

$\overline{CS}$ can be asserted (pulled high) after 16 clocks have elapsed. It is necessary not to start the next conversion by pulling $\overline{CS}$ low until the end of the quiet time (t_q) after SDO goes to 3-state. To continue normal operation, it is necessary that $\overline{CS}$ is not pulled high until point **b**. Without this, the device does not enter the acquisition phase and no valid data is available in the next cycle. (Also refer to power down mode for more details.) $\overline{CS}$ going high any time after the conversion start aborts the ongoing conversion and SDO goes to 3-state.

The high level of the digital input to the device is not limited to device V_{DD}. This means the digital input can go as high as 5.25 V when the device supply is 2.35 V. This feature is useful when digital signals are coming from another circuit with different supply levels. Also, this relaxes the restriction on power up sequencing. However, the digital output levels (V_{OH} and V_{OL}) are governed by V_{DD} as listed in the *Electrical Characteristics* table.

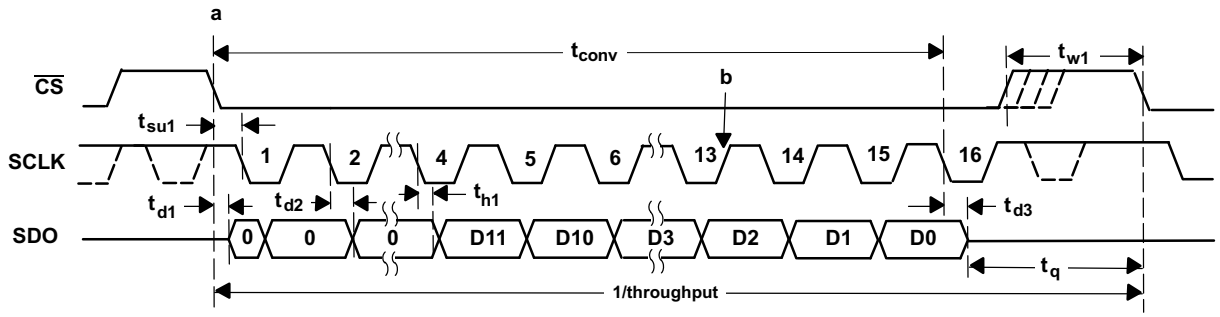


Figure 1. Interface Timing Diagram

POWER DOWN MODE

The device enters power down mode if $\overline{CS}$ goes high anytime after the 2nd SCLK falling edge to before the 10th SCLK falling edge. Ongoing conversion stops and SDO goes to 3-state under this power down condition as shown in Figure 2.

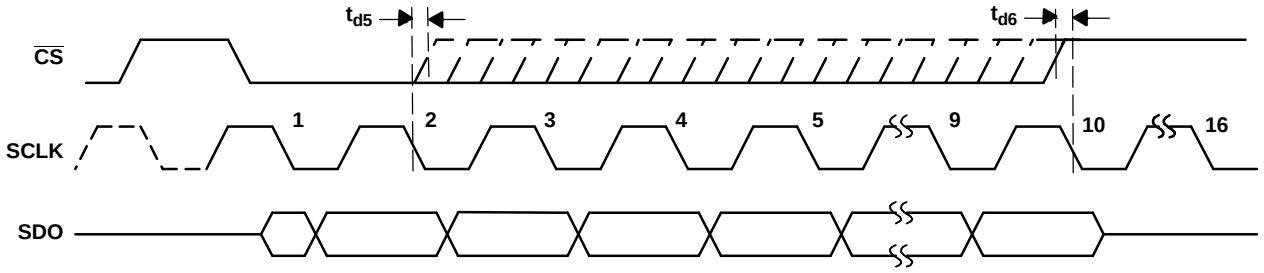


Figure 2. Entering Power Down Mode

A dummy cycle with $\overline{CS}$ low for more than 10 SCLK falling edges brings the device out of power down mode. For the device to come to the fully powered up condition it takes 1 µs. $\overline{CS}$ can be pulled high any time after the 10th falling edge as shown in Figure 3. It is not necessary to continue until the 16th clock if the next conversion starts 1 µs after $\overline{CS}$ going low of the dummy cycle and the quiet time (t_q) condition is met.

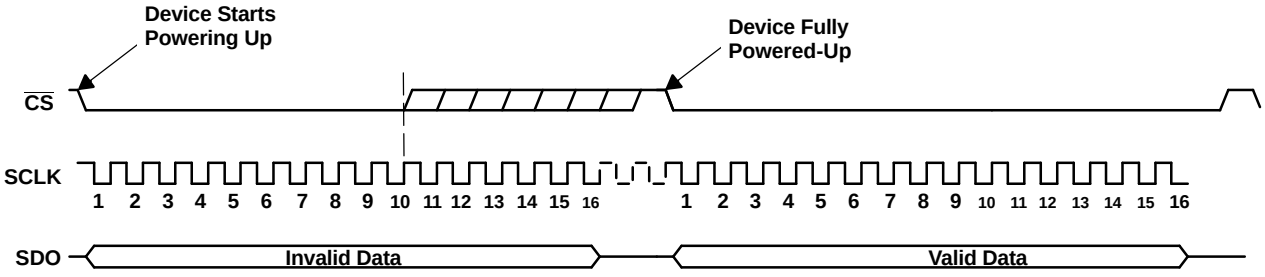


Figure 3. Exiting Power Down Mode

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

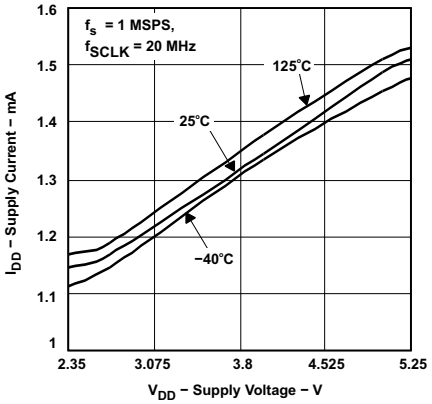


Figure 4.

SUPPLY CURRENT vs SCLK FREQUENCY

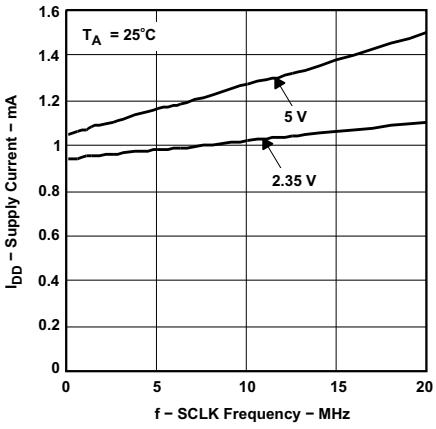


Figure 5.

SUPPLY CURRENT vs SAMPLE RATE

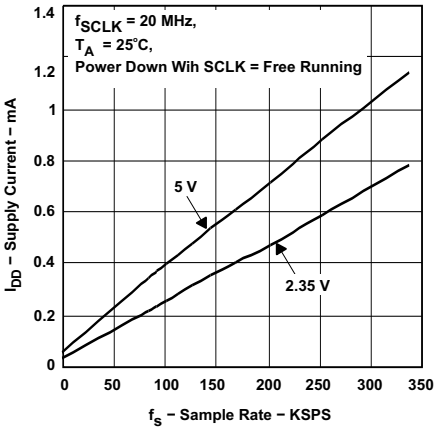


Figure 6.

ANALOG INPUT LEAKAGE CURRENT vs FREE-AIR TEMPERATURE

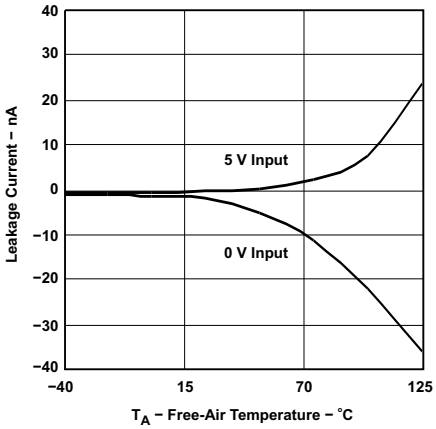


Figure 7.

TYPICAL CHARACTERISTICS

SIGNAL-TO-NOISE RATIO VS INPUT FREQUENCY

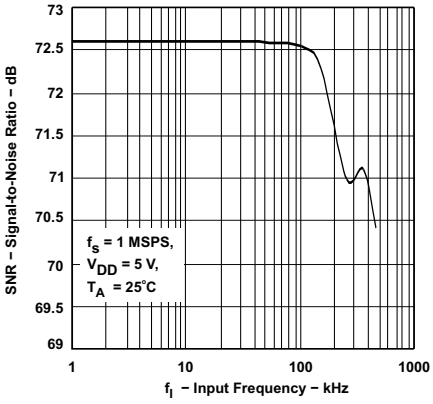


Figure 8.

SIGNAL-TO-NOISE RATIO VS SUPPLY VOLTAGE

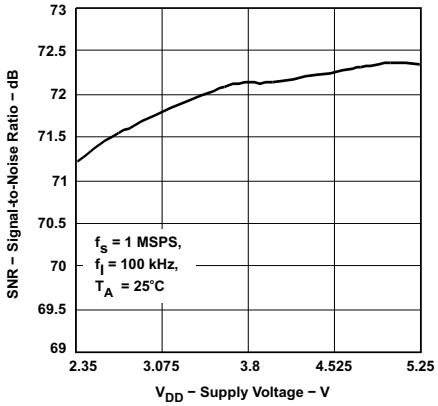


Figure 9.

SIGNAL-TO-NOISE RATIO VS FREE-AIR TEMPERATURE

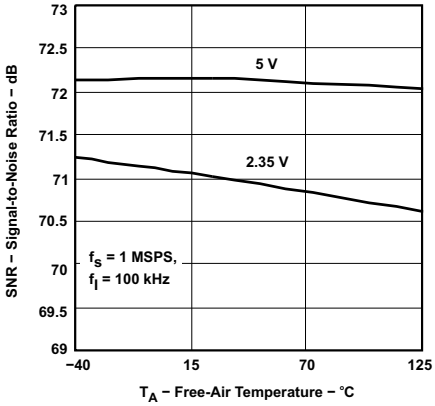


Figure 10.

TOTAL HARMONIC DISTORTION VS INPUT FREQUENCY

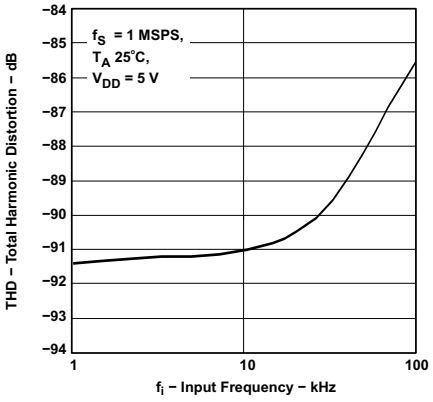


Figure 11.

TOTAL HARMONIC DISTORTION VS SUPPLY VOLTAGE

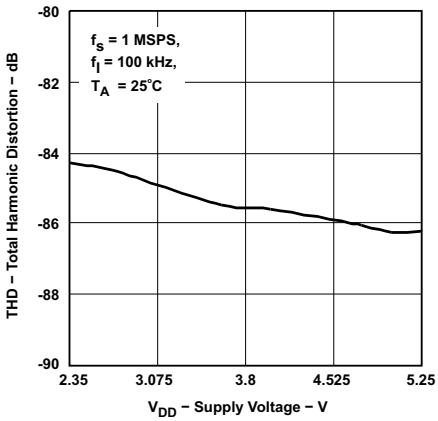


Figure 12.

TOTAL HARMONIC DISTORTION VS FREE-AIR TEMPERATURE

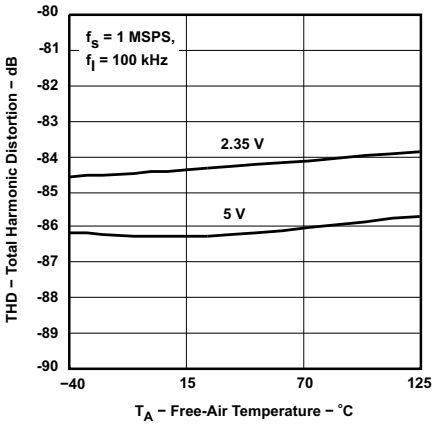


Figure 13.

SPURIOUS FREE DYNAMIC RANGE VS INPUT FREQUENCY

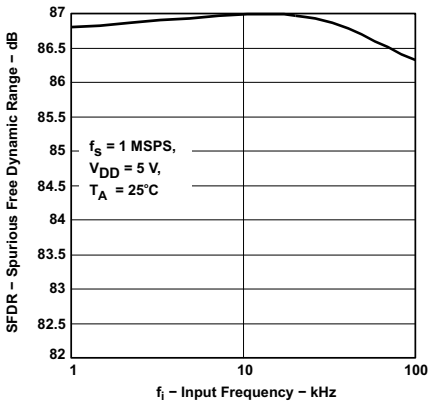


Figure 14.

SPURIOUS FREE DYNAMIC RANGE VS SUPPLY VOLTAGE

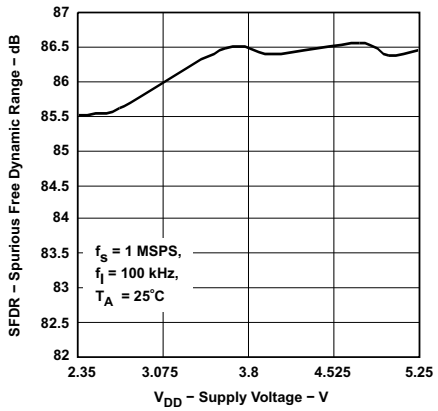


Figure 15.

SPURIOUS FREE DYNAMIC RANGE VS SUPPLY VOLTAGE

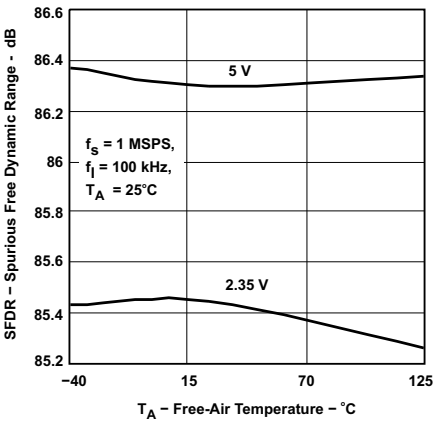


Figure 16.

TYPICAL CHARACTERISTICS (continued)

OFFSET ERROR VS SUPPLY VOLTAGE

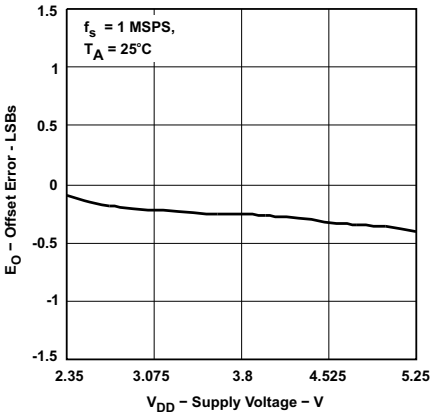


Figure 17.

OFFSET ERROR VS FREE-AIR TEMPERATURE

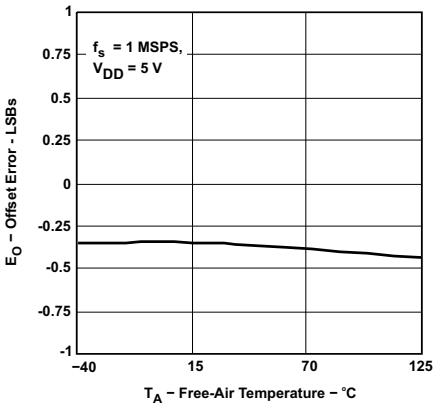


Figure 18.

GAIN ERROR VS SUPPLY VOLTAGE

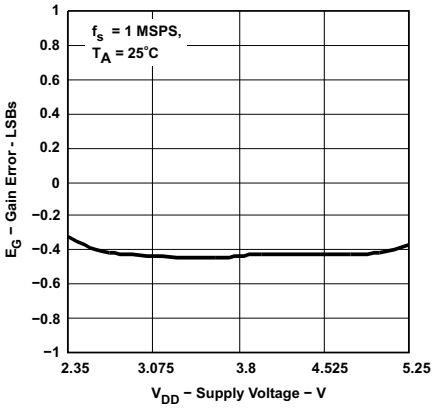


Figure 19.

GAIN ERROR VS FREE-AIR TEMPERATURE

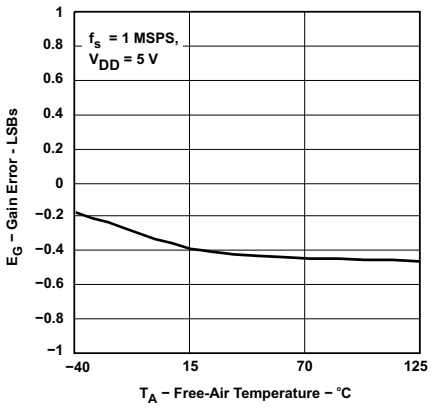


Figure 20.

DIFFERENTIAL LINEARITY ERROR VS SUPPLY VOLTAGE

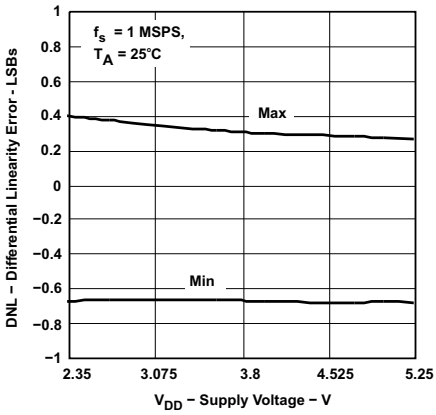


Figure 21.

DIFFERENTIAL NONLINEARITY VS FREE-AIR TEMPERATURE

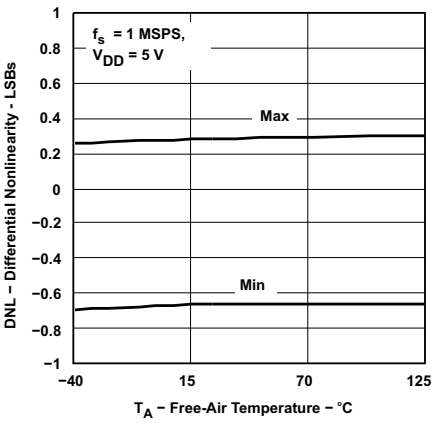


Figure 22.

INTEGRAL NONLINEARITY VS SUPPLY VOLTAGE

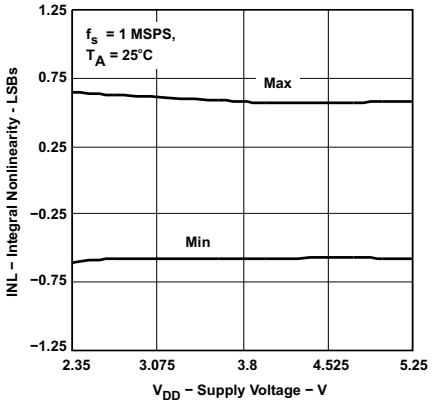


Figure 23.

INTEGRAL NONLINEARITY VS FREE-AIR TEMPERATURE

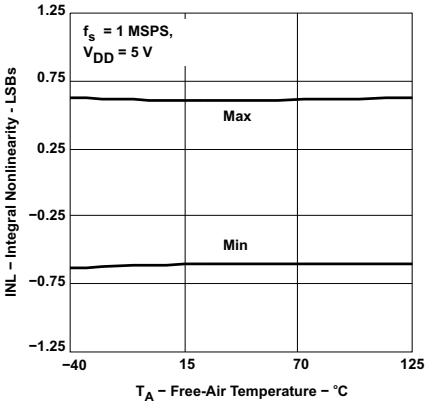


Figure 24.

TYPICAL CHARACTERISTICS (continued)

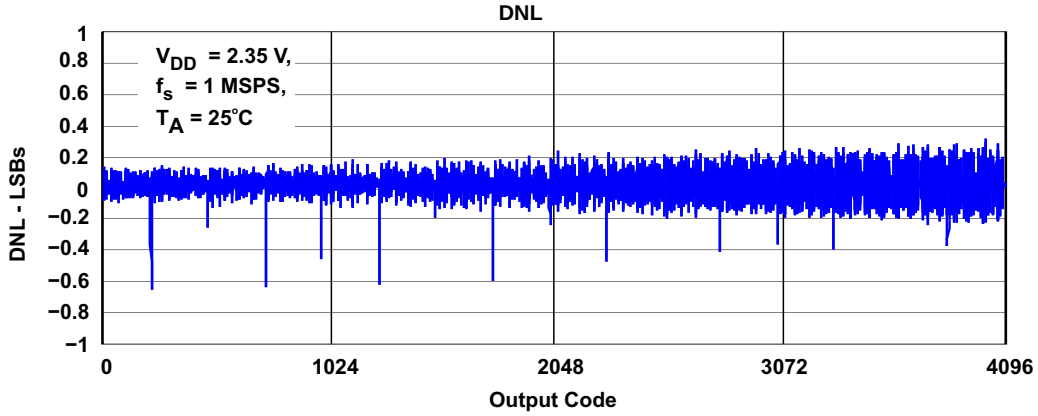


Figure 25.

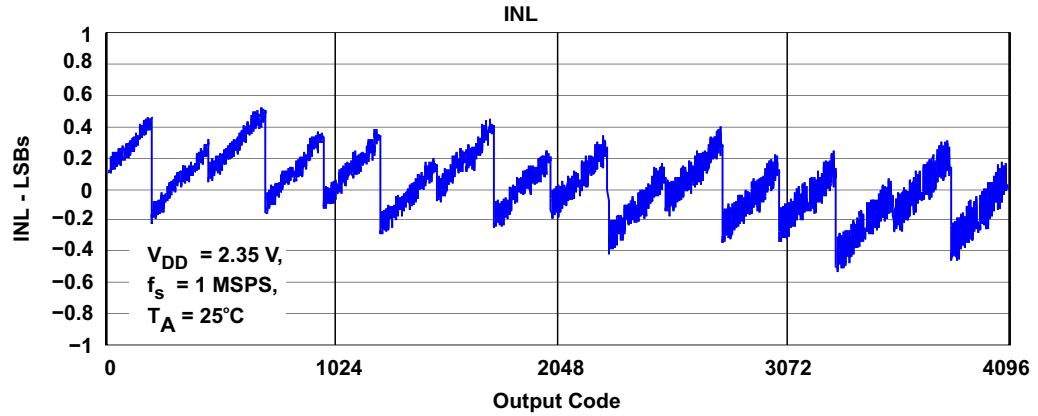


Figure 26.

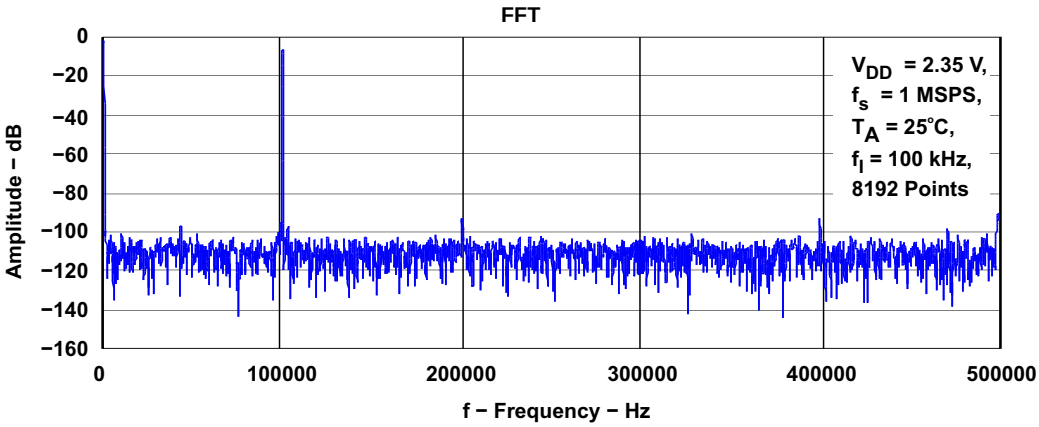


Figure 27.

APPLICATION INFORMATION

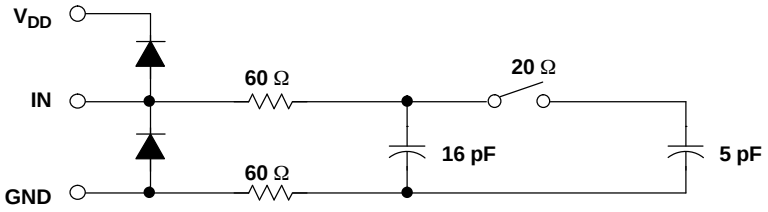


Figure 28. Typical Equivalent Sampling Circuit

Driving the VIN and V_{DD} Pins

The VIN input should be driven with a low impedance source. In most cases additional buffers are not required. In cases where the source impedance exceeds 200 Ω, using a buffer would help achieve the rated performance of the converter. The THS4031 is a good choice for the driver amplifier buffer.

The reference voltage for the A/D converter is derived from the supply voltage internally. The devices offer limited low-pass filtering functionality on-chip. The supply to these converters should be driven with a low impedance source and should be decoupled to the ground. A 1-µF storage capacitor and a 10-nF decoupling capacitor should be placed close to the device. Wide, low impedance traces should be used to connect the capacitor to the pins of the device. The ADS7886 draws very little current from the supply lines. The supply line can be driven by either:

- Directly from the system supply.
- A reference output from a low drift and low drop out reference voltage generator like REF3030 or REF3130. The ADS7886 operates from a wide range of supply voltages. The actual choice of the reference voltage generator would depend upon the system. Figure 30 shows one possible application circuit.
- A low-pass filtered system supply followed by a buffer, like the zero-drift OPA735, can also be used in cases where the system power supply is noisy. Care should be taken to ensure that the voltage at the V_{DD} input does not exceed 7 V to avoid damage to the converter. This can be done easily using single supply CMOS amplifiers like the OPA735. Figure 31 shows one possible application circuit.

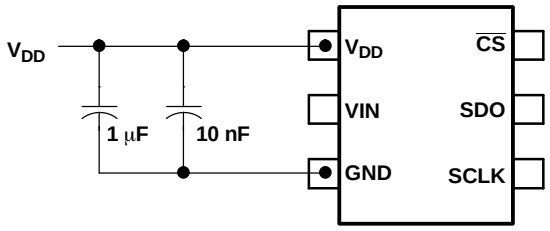


Figure 29. Supply/Reference Decoupling Capacitors

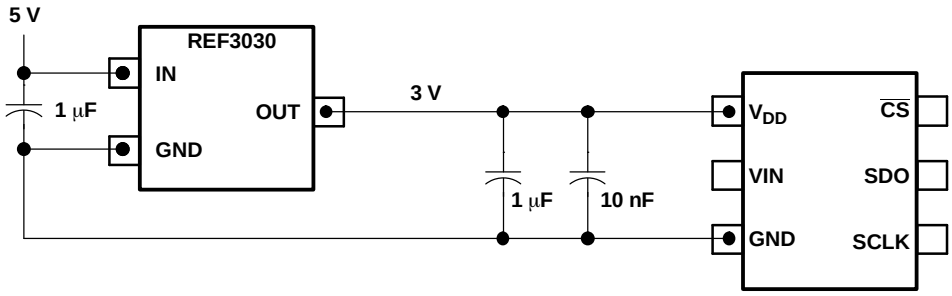


Figure 30. Using the REF3030 Reference

APPLICATION INFORMATION (continued)

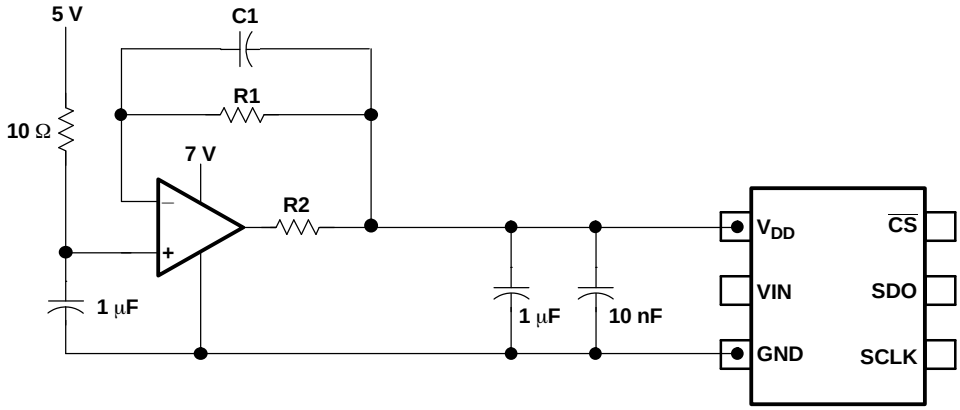


Figure 31. Buffering with the OPA735

PACKAGING INFORMATION

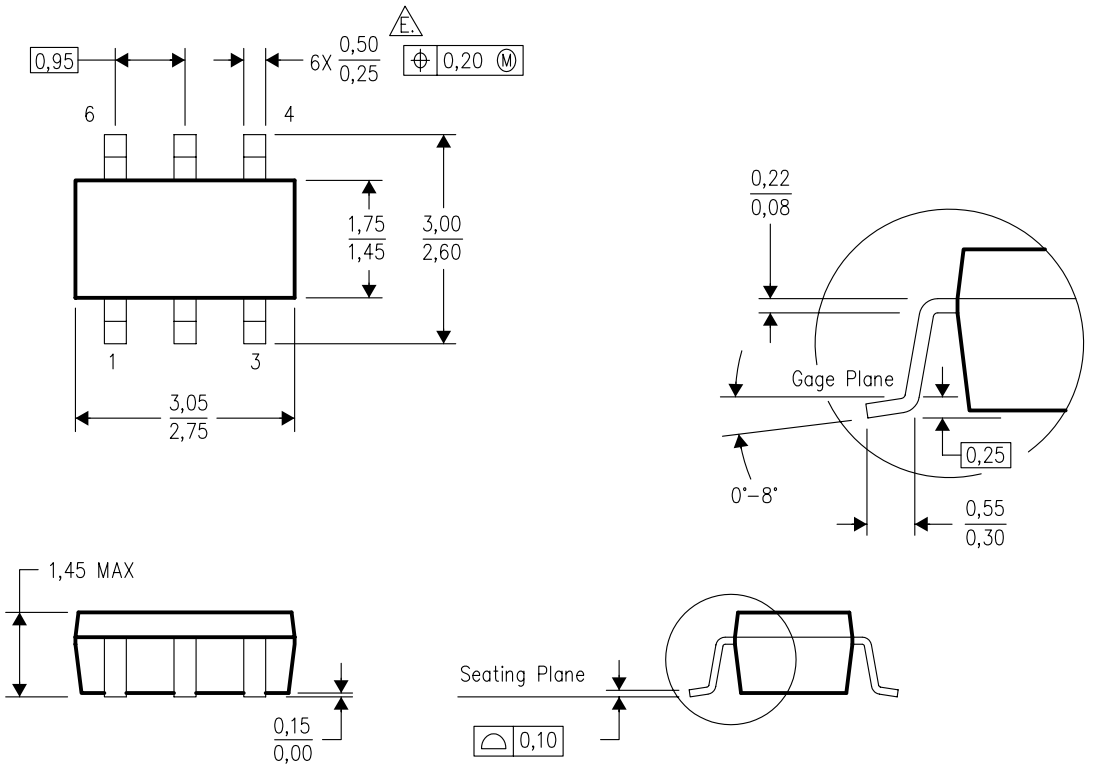
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS7886SBDBVR	ACTIVE	SOT-23	DBV	6	3000	TBD	CU SN	Level-2-260C-1 YEAR
ADS7886SBDBVT	ACTIVE	SOT-23	DBV	6	250	TBD	CU SN	Level-2-260C-1 YEAR
ADS7886SBDCKR	ACTIVE	SC70	DCK	6	3000	TBD	CU SN	Level-2-260C-1 YEAR
ADS7886SBDCKT	ACTIVE	SC70	DCK	6	250	TBD	CU SN	Level-2-260C-1 YEAR
ADS7886SDBVR	ACTIVE	SOT-23	DBV	6	3000	TBD	Call TI	Call TI
ADS7886SDBVT	ACTIVE	SOT-23	DBV	6	250	TBD	CU SN	Level-2-260C-1 YEAR
ADS7886SDCKR	ACTIVE	SC70	DCK	6	3000	TBD	Call TI	Call TI
ADS7886SDCKT	ACTIVE	SC70	DCK	6	250	TBD	CU SN	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

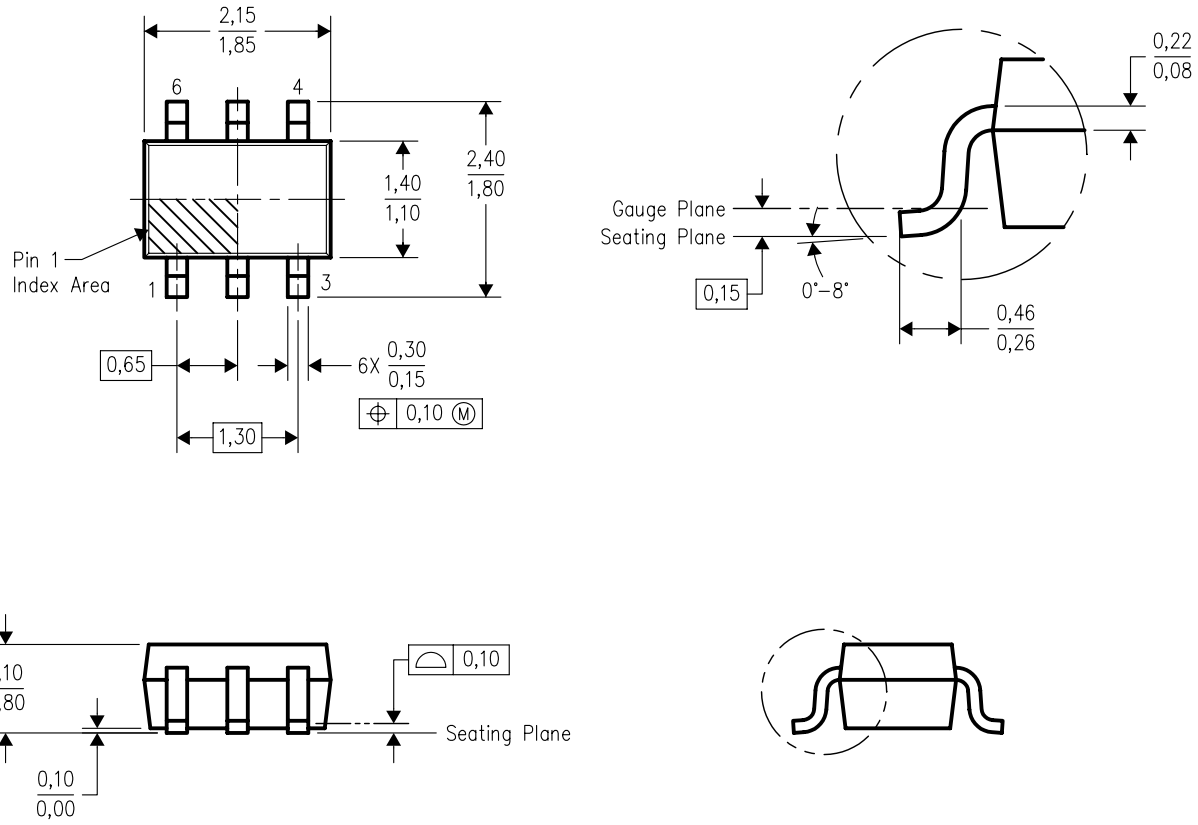
DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4073253–5/J 10/2005

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/E 10/2005

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

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