

STPIC6C595

Power logic 8-bit shift register

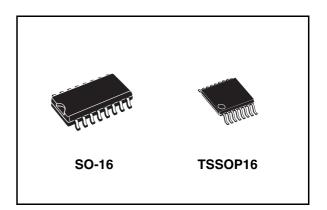
Features

- Low R_{DS(on)}: 4 Ω typ
- 30 mJ avalanche energy
- Eight 100 mA DMOS outputs
- 250 mA current limit capability
- 33 V output clamp voltage
- Device are cascadable
- Low power consumption

Description

This STPIC6C595 is a monolithic, mediumvoltage, low current power 8-bit shift register designed for use in systems that require relatively moderate load power such as LEDs. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other low-current or medium-voltage loads.

The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage register clock (SRCK) and the register clock (RCK), respectively. The device transfers data out the serial output (SER OUT) port on the rising edge of SRCK. The storage register transfers data to the output buffer when shift register clear (CLR) is high. When $\overline{\text{CLR}}$ is low, the input shift register is cleared. When output enable ($\overline{\text{G}}$) is held high, all data in the output buffer is held low and all drain output are off. When G is held low, data from the storage register is transparent to the output buffer.



When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability. The SER OUT allows for cascading of the data from the shift register to additional devices.

Output are low-side, open-drain DMOS transistors with output ratings of 33 V and 100 mA continuous sink-current capability. Each output provides a 250 mA maximum current limit at $T_C = 25$ °C. The current limit decreases as the junction temperature increases for additional device protection. The device also provides up to 1.5KV of ESD protection when tested using the human-body model and 150 V machine model.

The STPIC6C595 is characterized for operation over the operating case temperature range of -40 $^{\circ}$ C to 125 $^{\circ}$ C.

Table 1. Device summary

Order codes	Package	Packaging
STPIC6C595MTR	SO-16 (Tape and reel)	2500 parts per reel
STPIC6C595TTR	TSSOP16 (Tape and reel)	2500 parts per reel

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1 Logic symbol and pin configuration

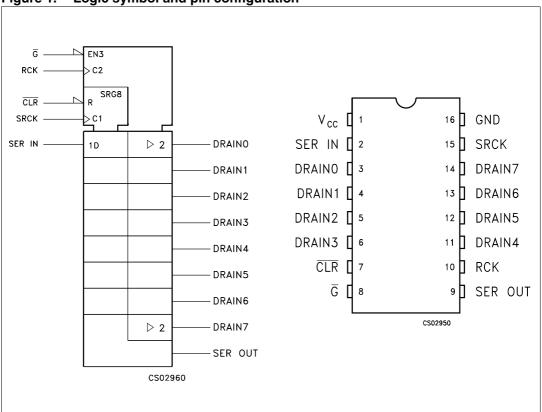
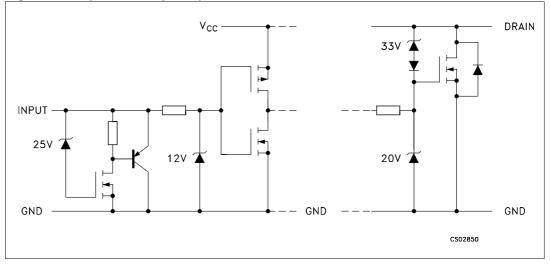


Figure 1. Logic symbol and pin configuration

Figure 2. Input and output equivalent circuits





2 Maximum rating

Stressing the device above the rating listed in the "absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

2.1 Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC}	Logic supply voltage (See Note 1)	7	V
VI	Logic input voltage range	-0.3 to 7	V
V _{DS}	Power DMOS drain to source voltage (See Note 2)	33	V
I _{DS}	Continuous source to drain diode anode current	250	mA
I _{DS}	Pulsed source to drain diode anode current (See <i>Note 3</i>)	500	mA
I _D	Pulsed drain current, each output, all output ON $(T_C = 25 \ ^{\circ}C)$	250	mA
I _D	Continuous current, each output, all output ON $(T_C = 25 \text{ °C})$	100	mA
I _D	Peak drain current single output (T _C = 25 °C) (See <i>Note 3</i>)	250	mA
E _{AS}	Single pulse avalanche energy (See <i>Figure 11</i> and <i>Figure 12</i>)	30	mJ
I _{AS}	Avalanche current (See <i>Note 4</i> and <i>Figure 17</i>)	200	mA
Pd	Continuous total dissipation (T _C \leq 25 °C)	1087	mW
Pd	Continuous total dissipation (T _C = 125 °C)	217	mW
TJ	Operating virtual junction temperature range	-40 to +150	°C
т _с	Operating case temperature range	-40 to +125	°C
T _{stg}	Storage temperature range	-65 to +150	°C
Τ _L	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260	°C

Table 2. Absolute maximum ratings



2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R _{th(JA)}	Thermal resistance junction-ambient	115	°C/W

2.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Min	Тур	Max	Unit
V _{CC}	Logic supply voltage	4.5		5.5	V
V _{IH}	High level input voltage	$0.85V_{CC}$		V _{CC}	V
V _{IL}	Low level input voltage	0		0.15V _{CC}	V
I _{DP}	Pulse drain output current ($T_C = 25 \text{ °C}, V_{CC} = 5 \text{ V}, \text{ all outputs ON}$) (see <i>Note 3</i> , <i>Note 5</i> and <i>Figure 15</i>)			250	mA
t _{su}	Set-up time, SER IN high before SRCK ↑ (see <i>Figure 4</i> and <i>Figure 8</i>)	1.6	3.0	5.7	ns
t _{hL}	Hold time, SER IN high before G ↑ (see <i>Figure 4, Figure 7, Figure 8</i>)	2.8	4.0	9.6	ns
t _W	Pulse duration (see <i>Figure 8</i>)	40			ns
T _C	Operating case temperature	-40		125	°C



3 Electrical characteristics

3.1 DC characteristics

Table 5. DC characteristics (V_{CC} = 5 V, T_C = 25 °C, unless otherwise specified.)

Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
V _{(BR)DSX}	Drain-to-source breakdown voltage	I _D = 1 mA	33	37		v
V _{SD}	Source-to-drain diode forward voltage	I _F = 100 mA		0.85	1.2	v
V _{OH}	High level output	I_{OH} = -20 μ A, V _{CC} = 4.5 V	4.4	4.49		V
VOH	voltage SER OUT	I _{OH} = -4 mA, V _{CC} = 4.5 V	4	4.2		V
V _{OL}	Low level output	I_{OH} = 20 μ A, V_{CC} = 4.5 V		0.005	0.1	V
♥OL	voltage SER OUT	I _{OH} = 4 mA, V _{CC} = 4.5 V		0.3	0.5	V
I _{IH}	High level input current	$V_{CC} = 5.5 \text{ V}, \text{ V}_{I} = V_{CC}$			1	μA
Ι _{ΙL}	Low level input current	$V_{CC} = 5.5 \text{ V}, \text{ V}_{I} = 0$			-1	μA
I _{CC}	Logic supply current	$V_{CC} = 5.5 \text{ V}$,all outputs OFF or ON		20	200	μA
I _{CC(FRQ)}	Logic supply current at frequency	$f_{SRCK} = 5 \text{ MHz}, C_L = 30 \text{ pF}$ All outputs OFF (See <i>Figure 6, Figure 18</i> and <i>Figure 19</i>)		0.2	2	mA
I _N	Nominal current	$V_{DS(on)} = 0.5 \text{ VI}_{N} = \text{I}_{D}$ T _C = 85 °C (See <i>Note 5, Note 6, Note 7</i>)		90		mA
		$V_{DS} = 30 \text{ V}, V_{CC} = 5.5 \text{ V}$		0.3	5	μA
I _{DSX}	Off-state drain current	$V_{DS} = 30 \text{ V}, V_{CC} = 5.5 \text{ V or } 0 \text{ V}$ $T_{C} = 125 \text{ °C}$		0.6	8	μA
	Static drain source on	$I_{D} = 50 \text{ mA}, V_{CC} = 4.5 \text{ V}$		4.5	6	w
R _{DS(on)}	state resistance (See <i>Note 5</i> , <i>Note 6</i> and <i>Figure 14</i> ,	$I_D = 50 \text{ mA}, V_{CC} = 4.5 \text{ V}$ $T_C = 125 \text{ °C}$		6.5	9	W
	Figure 16)	$I_{\rm D}$ = 100 mA, $V_{\rm CC}$ = 4.5 V		4.5	6	W



3.2 Switching characteristics

Table 6. Switching characteristics (V_{CC} = 5 V, T_C = 25 °C, unless otherwise specified.)

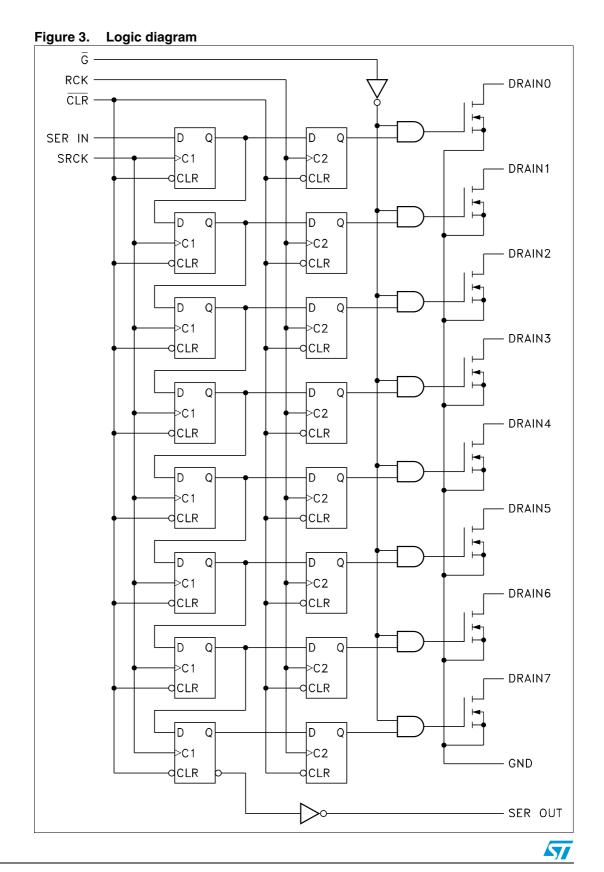
Symbol	Parameter Test conditions		Min	Тур	Max	Unit
t _{PHL}	Propagation delay time, high to low level output from \overline{G}			80		ns
t _{PLH}	Propagation delay time, low to high level output from \overline{G}	$C_L = 30 \text{ pF}, I_D = 75 \text{ mA}$ (See Figure 4, Figure 5,		130		ns
t _r	Rise time, drain output	Figure 6, Figure 7, Figure 20)		60		ns
t _f	Fall time, drain output			50		ns
t _{pd}	propagation delay time			20		ns
t _a	Reverse recovery current rise time	I _F = 100 mA, di/dt = 10 A/μs (See <i>Figure 5, Figure 6</i> , and		39		ns
t _{rr}	Reverse recovery time	Figure 9, Figure 10)		115		ns

Note: 1 All voltage value are with respect to GND

- 2 Each power DMOS source is internally connected to GND
- 3 Pulse duration \leq 100 μ s and duty cycle \leq 2 %
- 4 Drain supply voltage = 15 V, starting junction temperature $(T_{JS}) = 25 \text{ °C}$. L = 1.5 H and $I_{AS} = 200 \text{ mA}$ (see Fig. 11 and 12)
- 5 Technique should limit T_J T_C to 10 °C maximum
- 6 These parameters are measured with voltage sensing contacts separate from the currentcarrying contacts.
- 7 Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at $T_C = 85$ °C.

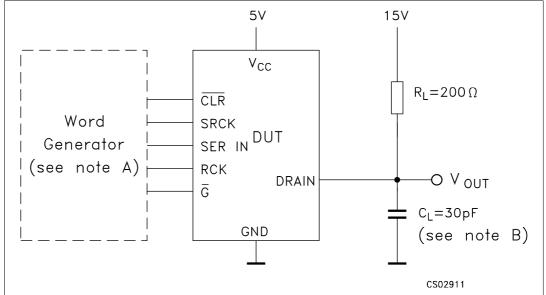


4 Logic diagram

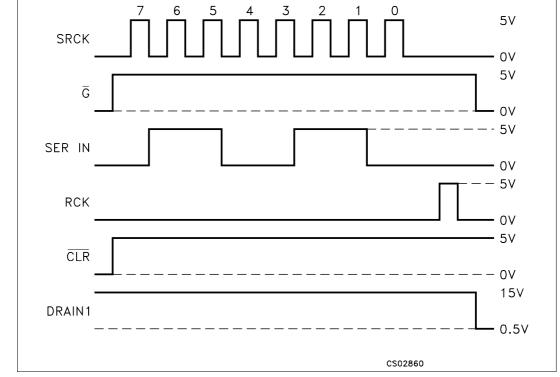


5 Typical operating circuit

Figure 4. Typical operation mode test circuits







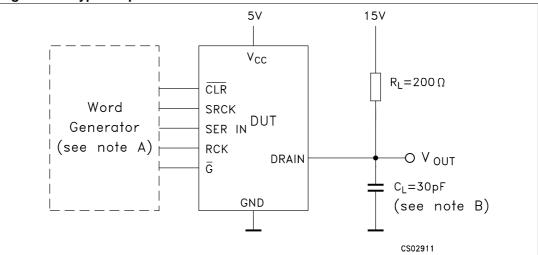
Note: 1 A) The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulse repetition rate (PRR) = 5 kHz, $Z_O = 50 \Omega$

2 B) C_L includes probe and jig capacitance.



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Figure 6. Typical operation mode test circuits





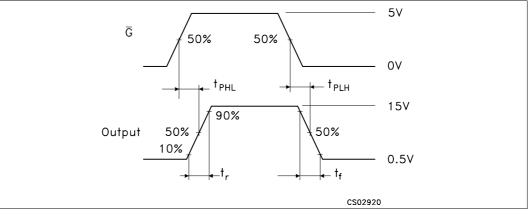
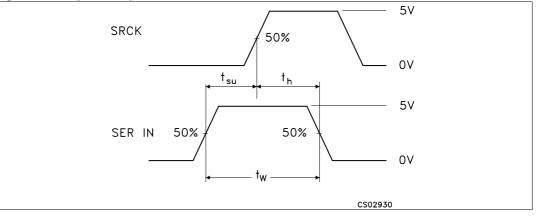


Figure 8. Input setup and hold waveform



Note: 1 A) The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulse repetition rate (PRR) = 5 kHz, $Z_O = 50 \Omega$

2 B) C_L includes probe and jig capacitance.

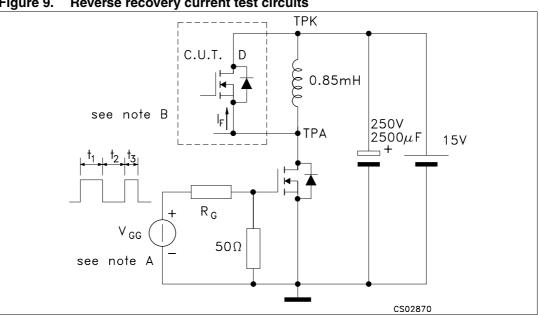
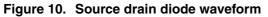
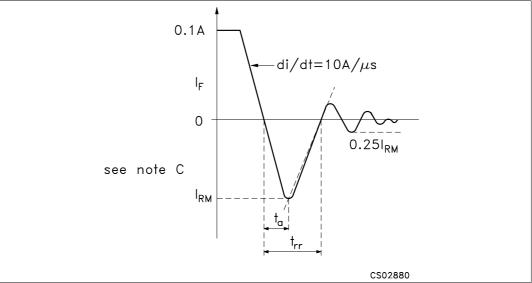


Figure 9. **Reverse recovery current test circuits**





- A) The V_{GG} amplitude and R_G are adjusted for di/dt = 10 A/ μ s. A V_{GG} double-pulse train is Note: 1 used to set $I_F = 0.1$ A. where $t_1 = 10 \ \mu s$, $t_2 = 7 \ \mu s$ and $t_3 = 3 \ \mu s$
 - 2 B) The drain terminal under test is connected to the TPK test point. All other terminals are connected together and connected to the TPA test point.
 - 3 C) I_{RM} = maximum recovery current.



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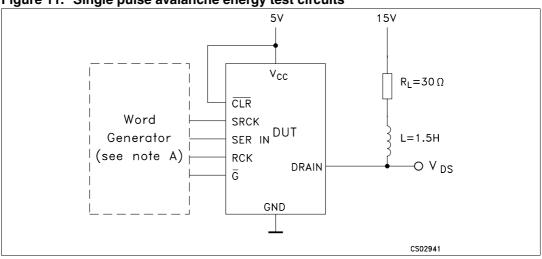
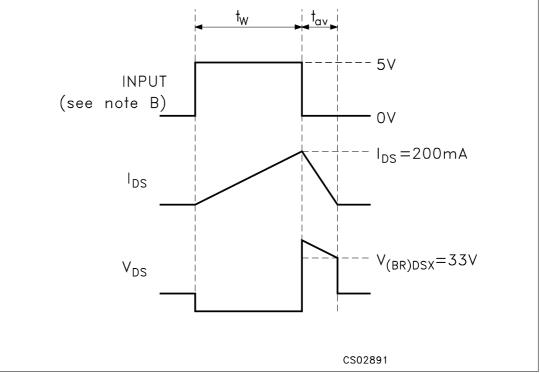


Figure 11. Single pulse avalanche energy test circuits





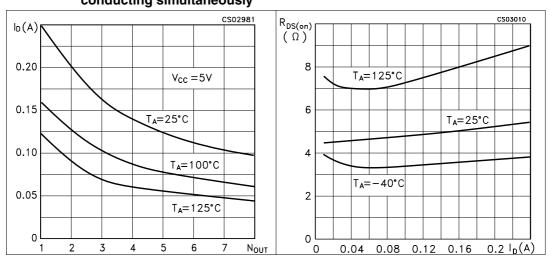
- Note: 1 A) The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_0 = 50 \Omega$
 - *B)* Input pulse duration, t_W is increased until peak current $I_{AS} = 200$ mA. Energy test level is defined as $E_{AS} = (I_{AS} \times V_{(BR)DSX} \times t_{AV})/2 = 30$ mJ.

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6 Typical performance and characteristics

(unless otherwise specified $T_J = 25 \ ^{\circ}C$)

Figure 13. Max continuous drain current Figure 14. Static drain-source on-state vs number of outputs resistance vs drain current conducting simultaneously



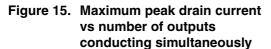
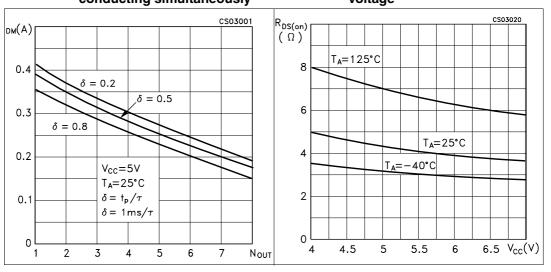


Figure 16. Static drain-source on-state resistance vs logic supply voltage



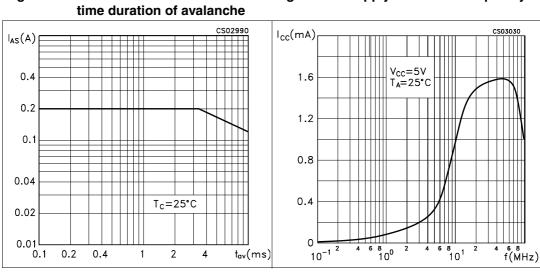
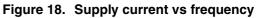


Figure 17. Peak avalanche current vs



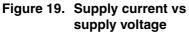
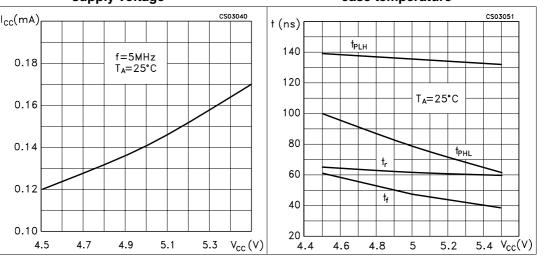


Figure 20. Switching time vs case temperature





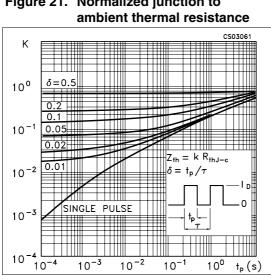


Figure 21. Normalized junction to

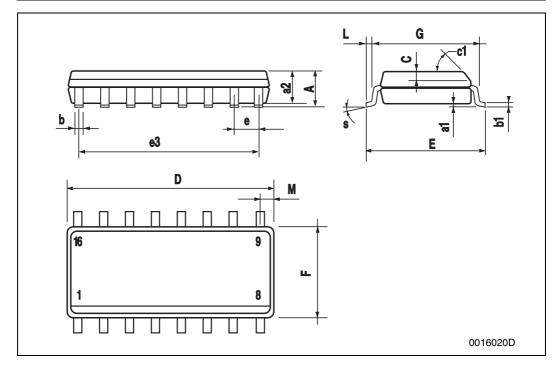


7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

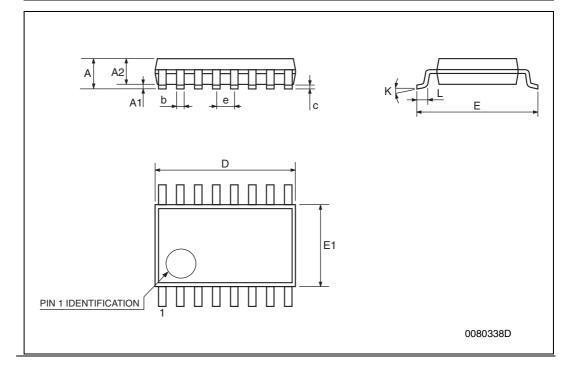


SO-16 MECHANICAL DATA						
DIM.		mm.				
DIM.	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX.
А			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
С		0.5			0.019	
c1			45°	(typ.)	•	
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
е		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
М			0.62			0.024
S			8° (r	nax.)	•	



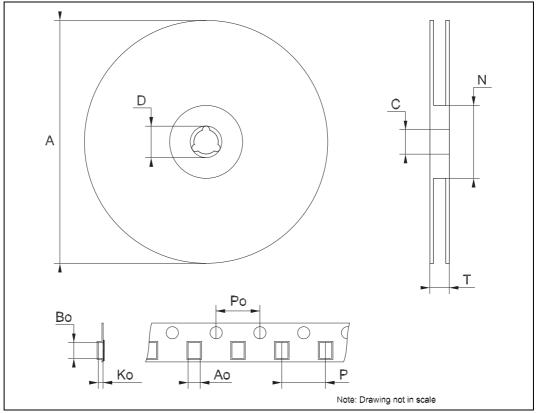


	TSSOP16 MECHANICAL DATA							
DIM.		mm.		inch				
Diwi.	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX.		
А			1.2			0.047		
A1	0.05		0.15	0.002	0.004	0.006		
A2	0.8	1	1.05	0.031	0.039	0.041		
b	0.19		0.30	0.007		0.012		
С	0.09		0.20	0.004		0.0079		
D	4.9	5	5.1	0.193	0.197	0.201		
E	6.2	6.4	6.6	0.244	0.252	0.260		
E1	4.3	4.4	4.48	0.169	0.173	0.176		
е		0.65 BSC			0.0256 BSC			
к	0°		8°	0°		8°		
L	0.45	0.60	0.75	0.018	0.024	0.030		

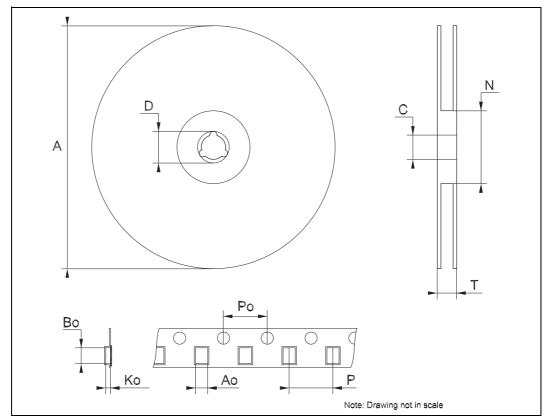




Tape & Reel SO-16 MECHANICAL DATA							
DIM		mm.		inch			
DIM.	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX.	
А			330			12.992	
С	12.8		13.2	0.504		0.519	
D	20.2			0.795			
Ν	60			2.362			
Т			22.4			0.882	
Ao	6.45		6.65	0.254		0.262	
Во	10.3		10.5	0.406		0.414	
Ko	2.1		2.3	0.082		0.090	
Po	3.9		4.1	0.153		0.161	
Р	7.9		8.1	0.311		0.319	



DIM		mm.			inch	
DIM.	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX.
А			330			12.992
С	12.8		13.2	0.504		0.519
D	20.2			0.795		
Ν	60			2.362		
Т			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Во	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
Р	7.9		8.1	0.311		0.319





8 Revision history

Table 7. Document revision history

Date	Revision	Changes
07-Jul-2004	2	Update Figure 3
07-May-2007	3	Document reformatted, tube package deleted
21-May-2008	4	Update: tsu and ThL values in <i>Table 4</i> , ESD value on cover page



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