FLATLINK™ TRANSMITTER

Check for Samples: SN65LVDS93A

FEATURES

- **Industrial Temperature Range –40°C to 85°C**
- **LVDS Display Serdes Interfaces Directly to LCD Display Panels with Integrated LVDS**
- **Package Options: 4.5mm × 7mm BGA, and 8.1mm × 14mm TSSOP**
- **1.8V up to 3.3V Tolerant Data Inputs to Connect Directly to Low-Power, Low-Voltage Application and Graphic Processors**
- **Transfer Rate up to 135Mpps (Mega Pixel Per Second); Pixel Clock Frequency Range 10MHz to 135MHz**
- **Suited for Display Resolutions Ranging From HVGA up to HD With Low EMI**
- **Operates From a Single 3.3V Supply and 170mW (typ.) at 75MHz**

- **28 Data Channels Plus Clock In Low-Voltage TTL to 4 Data Channels Plus Clock Out Low-Voltage Differential**
- **Consumes Less Than 1mW When Disabled**
- **Selectable Rising or Falling Clock Edge Triggered Inputs**
- **ESD: 5kV HBM**
- **Support Spread Spectrum Clocking (SSC)**
- **Compatible with all OMAP ™ 2x, OMAP™3x, and DaVinci ™ Application Processors**

APPLICATIONS

- **LCD Display Panel Driver**
- **UMPC and Netbook PC**
- **Digital Picture Frame**

DESCRIPTION

The SN65LVDS93A LVDS serdes (serializer/deserializer) transmitter contains four 7-bit parallel load serial-out shift registers, a 7 × clock synthesizer, and five low-voltage differential signaling (LVDS) drivers in a single integrated circuit. These functions allow 28 bits of single-ended LVTTL data to be synchronously transmitted over five balanced-pair conductors for receipt by a compatible receiver, such as the SN65LVDS94.

When transmitting, data bits D0 through D27 are each loaded into registers upon the edge of the input clock signal (CLKIN). The rising or falling edge of the clock can be selected via the clock select (CLKSEL) pin. The frequency of CLKIN is multiplied seven times and then used to serially unload the data registers in 7-bit slices. The four serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

The SN65LVDS93A requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is selecting a clock rising edge by inputting a high level to CLKSEL or a falling edge with a lowlevel input and the possible use of the shutdown/clear (SHTDN). SHTDN is an active-low input to inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low level on this signal clears all internal registers at a low level.

The SN65LVDS93A is characterized for operation over ambient air temperatures of –40°C to 85°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION[1]

PART NUMBER	PART MARKING	PACKAGE
SN65LVDS93AZQLR	LVDS93A in BGA package	56-pin ZQL LARGE T&R
SN65LVDS93ADGG	LVDS93A in TSSOP package	56-pin DGG TUBE
SN65LVDS93ADGGR	LVDS93A in TSSOP package	56-pin DGG LARGE T&R

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS[1]

		VALUE	UNIT
Supply voltage range, VCC, IOVCC, LVDSVCC, PLLVCC[2]		-0.5 to 4	V
Voltage range at any output terminal		-0.5 to VCC + 0.5	V
Voltage range at any input terminal		-0.5 to IOVCC + 0.5	V
Continuous power dissipation		See the dissipation rating table	
ESD rating	Human Body Model (HBM)[3] all pins	5	kV
	Charged Device Model (CDM)[4] all pins	500	V
	Machine Model (MM)[5] all pins	150	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) All voltages are with respect to the GND terminals.
(3) In accordance with JEDEC Standard 22, Test Method A114-A.
(4) In accordance with JEDEC Standard 22, Test Method C101.
(5) In accordance with JEDEC Standard 22, Test Method A115-A.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, VCC		3	3.3	3.6	
LVDS output Supply voltage, LVDSVCC		3	3.3	3.6	
PLL analog supply voltage, PLLVCC		3	3.3	3.6	V
IO input reference Supply voltage, IOVCC		1.62	1.8 / 2.5 / 3.3	3.6	
Power supply noise on any VCC terminal				0.1	
High-level input voltage, V_{IH}	IOVCC = 1.8V	IOVCC/2 + 0.3V			
	IOVCC = 2.5V	IOVCC/2 + 0.4V			V
	IOVCC = 3.3V	IOVCC/2 + 0.5V			
Low-level input voltage, V_{IL}	IOVCC = 1.8V			IOVCC/2 - 0.3V	
	IOVCC = 2.5V			IOVCC/2 - 0.4V	V
	IOVCC = 3.3V			IOVCC/2 - 0.5V	
Differential load impedance, Z_L		90		132	Ω
Operating free-air temperature, T_A		-45		85	C

DISSIPATION RATINGS

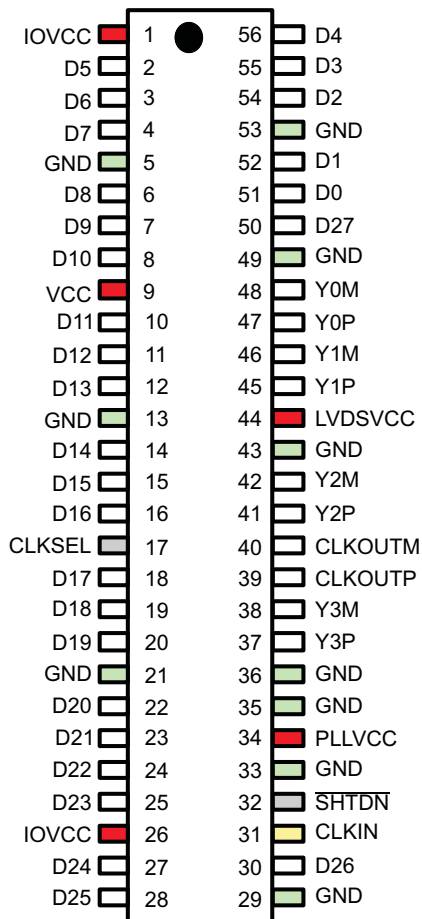| PACKAGE	CIRCUIT BOARD MODEL [1]	T_{JA} ≤ 25°C	DERATING FACTOR [2] ABOVE T_{JA} = 25°C	T_{JA} = 70°C POWER RATING
DGG	Low-K	1111mW	12.3mW/°C	555mW
ZQL		1034mW	11.5mW/°C	517mW
DGG	High-K	1730mW	19mW/°C	865mW
ZQL		2000mW	22mW/°C	1000mW

(1) In accordance with the High-K and Low-K thermal metric definitions of EIA/JESD51-2.
(2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

TIMING REQUIREMENTS

PARAMETER	MIN	MAX	UNIT
Input clock period, t_c	7.4	100	ns
Input clock modulation			
w/ modulation frequency 30kHz		8%	
w/ modulation frequency 50kHz		6%	
High-level input clock pulse width duration, t_w	0.4 t_c	0.6 t_c	ns
Input signal transition time, t_t		3	ns
Data set up time, D0 through D27 before CLKIN (See Figure 3)	2		ns
Data hold time, D0 through D27 after CLKIN	0.8		ns

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DGG PACKAGE
(TOP VIEW)

IOVCC	1	56	D4
D5	2	55	D3
D6	3	54	D2
D7	4	53	GND
GND	5	52	D1
D8	6	51	D0
D9	7	50	D27
D10	8	49	GND
VCC	9	48	Y0M
D11	10	47	Y0P
D12	11	46	Y1M
D13	12	45	Y1P
GND	13	44	LVDSVCC
D14	14	43	GND
D15	15	42	Y2M
D16	16	41	Y2P
CLKSEL	17	40	CLKOUTM
D17	18	39	CLKOUTP
D18	19	38	Y3M
D19	20	37	Y3P
GND	21	36	GND
D20	22	35	GND
D21	23	34	PLLVCC
D22	24	33	GND
D23	25	32	$\overline{\text{SHTDN}}$
IOVCC	26	31	CLKIN
D24	27	30	D26
D25	28	29	GND

DGG PIN LIST

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1	IOVCC	15	D15	29	GND	43	GND
2	D5	16	D16	30	D26	44	LVDSVCC
3	D6	17	CLKSEL	31	CLKIN	45	Y1P
4	D7	18	D17	32	$\overline{\text{SHTDN}}$	46	Y1M
5	GND	19	D18	33	GND	47	Y0P
6	D8	20	D19	34	PLLVCC	48	Y0M
7	D9	21	GND	35	GND	49	GND
8	D10	22	D20	36	GND	50	D27
9	VCC	23	D21	37	Y3P	51	D0
10	D11	24	D22	38	Y3M	52	D1
11	D12	25	D23	39	CLKOUTP	53	GND
12	D13	26	IOVCC	40	CLKOUTM	54	D2
13	GND	27	D24	41	Y2P	55	D3
14	D14	28	D25	42	Y2M	56	D4

Product Folder Link(s): *SN65LVDS93A*

ZQL PACKAGE
(TOP VIEW)
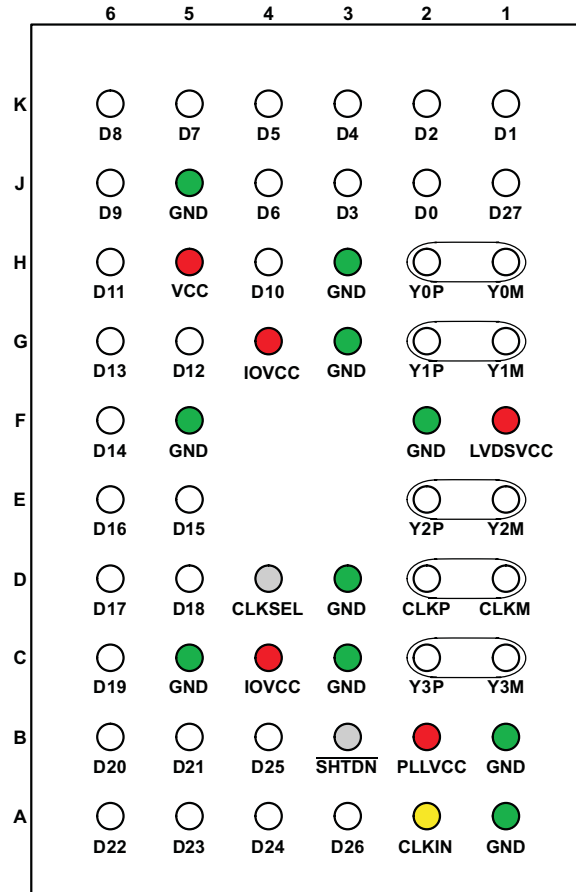
ZQL PIN LIST

Ball #	Signal	Ball #	Signal	Ball #	Signal
A1	GND	A2	CLKIN	A3	D26
A4	D24	A5	D23	A6	D22
B1	GND	B2	PLLVCC	B3	SHTDN
B4	D25	B5	D21	B6	D20
C1	Y3M	C2	Y3P	C3	GND
C4	IOVCC	C5	GND	C6	D19
D1	CLKM	D2	CLKP	D3	GND
D4	CLKSEL	D5	D18	D6	D17
E1	Y2M	E2	Y2P	E3	ball not populated
E4	ball not populated	E5	D15	E6	D16
F1	LVDSVCC	F2	GND	F3	ball not populated
F4	ball not populated	F5	GND	F6	D14
G1	Y1M	G2	Y1P	G3	GND
G4	IOVCC	G5	D12	G6	D13
H1	Y0M	H2	Y0P	H3	GND
H4	D10	H5	VCC	H6	D11
J1	D27	J2	D0	J3	D3
J4	D6	J5	GND	J6	D9
K1	D1	K2	D2	K3	D4
K4	D5	K5	D7	K6	D8

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PIN FUNCTIONS

PIN	I/O	DESCRIPTION
Y0P, Y0M, Y1P, Y1M, Y2P, Y2M	LVDS Out	Differential LVDS data outputs. Outputs are high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted)
Y3P, Y3M		Differential LVDS Data outputs. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted). Note: if the application only requires 18-bit color, this output can be left open.
CLKP, CLKM		Differential LVDS pixel clock output. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted).
D0 – D27	CMOS IN with pulldn	Data inputs; supports 1.8V to 3.3V input voltage selectable by VDD supply. To connect a graphic source successfully to a display, the bit assignment of D[27:0] is critical (and not necessarily intuitive). Note: if application only requires 18-bit color, connect unused inputs D5, D10, D11, D16, D17, D23, and D27 to GND.
CLKIN		Input pixel clock; rising or falling clock polarity is selectable by Control input CLKSEL.
$\overline{\text{SHTDN}}$		Device shut down; pull low (de-assert) to shut down the device (low power, resets all registers) and high (assert) for normal operation.
CLKSEL		Selects between rising edge input clock trigger (CLKSEL = V_{IH} and falling edge input clock trigger (CLKSEL = V_{IL}).
VCC	Power Supply[1]	3.3V digital Supply Voltage
IOVCC		I/O supply reference voltage (1.8V up to 3.3V matching the GPU data output signal swing)
PLLVCC		3.3V PLL analog supply
LVDSVCC		3.3V LVDS output analog supply
GND		Supply Ground for VCC, IOVCC, LVDSVCC, and PLLVCC.

(1)   For a multilayer pcb, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

Product Folder Link(s): *SN65LVDS93A*

FUNCTIONAL BLOCK DIAGRAM
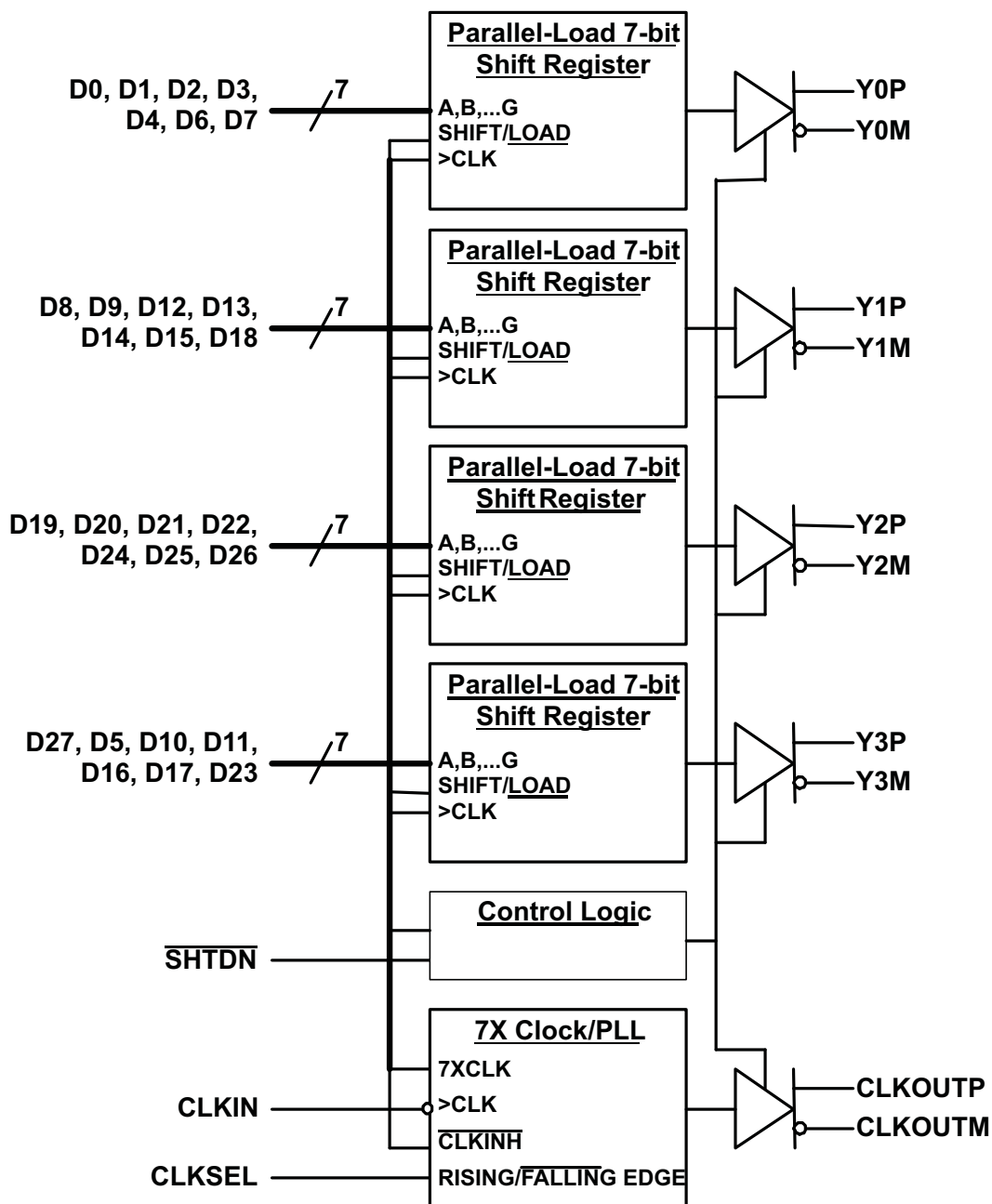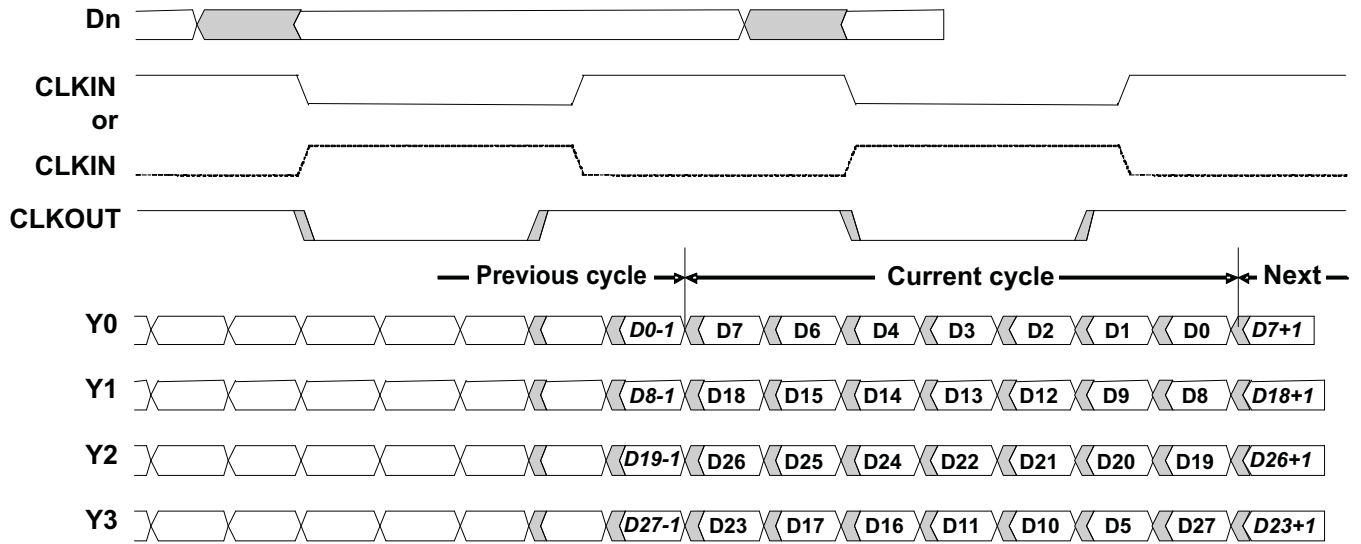
SN65LVDS93A

Figure 1. Typical SN65LVDS93A Load and Shift Sequences
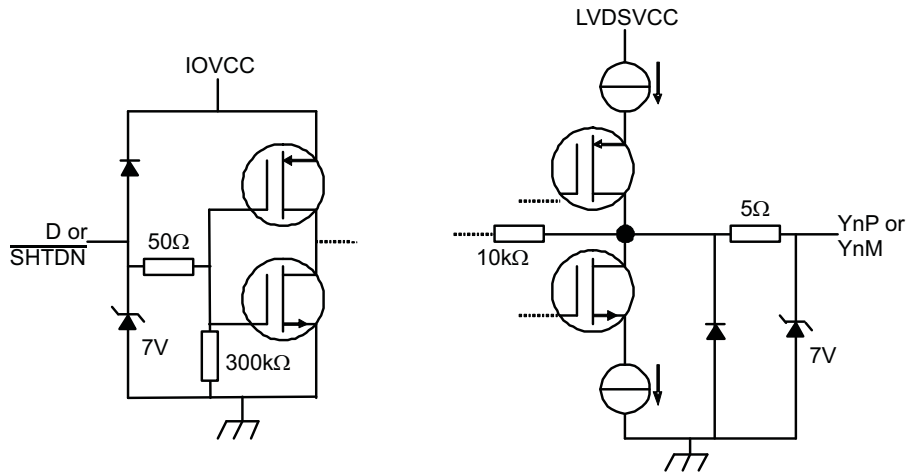
Figure 2. Equivalent Input and Output Schematic Diagrams

Product Folder Link(s): *SN65LVDS93A*

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
V_T	Input voltage threshold			IOVCC/2		V
$|V_{OD}|$	Differential steady-state output voltage magnitude	R_L = 100Ω, See Figure 4	250		450	mV
$\Delta|V_{OD}|$	Change in the steady-state differential output voltage magnitude between opposite binary states			1	35	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 4 $t_{R/F}$ (Dx, CLKin) = 1ns	1.125		1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				35	mV
I_{IH}	High-level input current	V_{IH} = IOVCC			25	µA
I_{IL}	Low-level input current	V_{IL} = 0 V			±10	µA
I_{OS}	Short-circuit output current	V_{OY} = 0 V			±24	mA
		V_{OD} = 0 V			±12	mA
I_{OZ}	High-impedance state output current	V_O = 0 V to VCC			±20	µA
R_{pdn}	Input pull-down integrated resistor on all inputs (Dx, CLKSEL, $\overline{SHTDN}$, CLKIN)	IOVCC = 1.8V		200		kΩ
		IOVCC = 3.3V		100		
I_Q	Quiescent current	disabled, all inputs at GND; $\overline{SHTDN}$ = V_{IL}		2	100	µA
I_{CC}	Supply current (average)	$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), grayscale pattern (Figure 5) VCC = 3.3V, f_{CLK} = 75MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		51.9	62	mA
		$I_{(IOVCC)}$ with IOVCC = 3.3V		0.4	1.2	
		$I_{(IOVCC)}$ with IOVCC = 1.8V		0.1		
		$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), 50% transition density pattern (Figure 5), VCC = 3.3V, f_{CLK} = 75MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		53.3	65	mA
		$I_{(IOVCC)}$ with IOVCC = 3.3V		0.6	2.5	
		$I_{(IOVCC)}$ with IOVCC = 1.8V		0.2		
		$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), worst-case pattern (Figure 6), VCC = 3.6V, f_{CLK} = 75MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		63.7	77	mA
		$I_{(IOVCC)}$ with IOVCC = 3.3V		1.3	3.3	
		$I_{(IOVCC)}$ with IOVCC = 1.8V		0.5		
		$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), worst-case pattern (Figure 6), f_{CLK} = 100MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		81.6	94	mA
		$I_{(IOVCC)}$ with IOVCC = 3.6V		1.6	3.8	
		$I_{(IOVCC)}$ with IOVCC = 1.8V		0.6		
		$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), worst-case pattern (Figure 6), f_{CLK} = 135MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		102.2	116	mA
		$I_{(IOVCC)}$ with IOVCC = 3.6V		2.1	4.5	
		$I_{(IOVCC)}$ with IOVCC = 1.8V		0.8		
C_I	Input capacitance			2		pF

(1)   All typical values are at VCC = 3.3 V, T_A = 25°C.

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SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
t_0	Delay time, CLKOUT↑ after Yn valid (serial bit position 0, equal D1, D9, D20, D5)	See Figure 7, t_C = 10ns, |Input clock jitter| < 25ps [2]	-0.1	0	0.1	ns
t_1	Delay time, CLKOUT↑ after Yn valid (serial bit position 1, equal D0, D8, D19, D27)		$^1/_7\, t_c$ - 0.1		$^1/_7\, t_c$ + 0.1	ns
t_2	Delay time, CLKOUT↑ after Yn valid (serial bit position 2, equal D7, D18, D26. D23)		$^2/_7\, t_c$ - 0.1		$^2/_7\, t_c$ + 0.1	ns
t_3	Delay time, CLKOUT↑ after Yn valid (serial bit position 3; equal D6, D15, D25, D17)		$^3/_7\, t_c$ - 0.1		$^3/_7\, t_c$ + 0.1	ns
t_4	Delay time, CLKOUT↑ after Yn valid (serial bit position 4, equal D4, D14, D24, D16)		$^4/_7\, t_c$ - 0.1		$^4/_7\, t_c$ + 0.1	ns
t_5	Delay time, CLKOUT↑ after Yn valid (serial bit position 5, equal D3, D13, D22, D11)		$^5/_7\, t_c$ - 0.1		$^5/_7\, t_c$ + 0.1	ns
t_6	Delay time, CLKOUT↑ after Yn valid (serial bit position 6, equal D2, D12, D21, D10)		$^6/_7\, t_c$ - 0.1		$^6/_7\, t_c$ + 0.1	ns
$t_{c(o)}$	Output clock period			t_c		ns
$\Delta t_{c(o)}$	Output clock cycle-to-cycle jitter [3]	t_C = 10ns; clean reference clock, see Figure 8		±26		ps
		t_C = 10ns with 0.05UI added noise modulated at 3MHz, see Figure 8		±44		
		t_C = 7.4ns; clean reference clock, see Figure 8		±35		
		t_C = 7.4ns with 0.05UI added noise modulated at 3MHz, see Figure 8		±42		
t_w	High-level output clock pulse duration			$^4/_7\, t_c$		ns
$t_{r/f}$	Differential output voltage transition time (t_r or t_f)	See Figure 4		225	500	ps
t_{en}	Enable time, $\overline{\text{SHTDN}}$↑ to phase lock (Yn valid)	$f_{(clk)}$ = 135MHz, See Figure 9		6		ns
t_{dis}	Disable time, $\overline{\text{SHTDN}}$↓ to off-state (CLKOUT high-impedance)	$f_{(clk)}$ = 135MHz, See Figure 10		7		ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) |Input clock jitter| is the magnitude of the change in the input clock period.
(3) The output clock cycle-to-cycle jitter is the largest recorded change in the output clock period from one cycle to the next cycle observed over 15,000 cycles. Tektronix TDSJIT3 Jitter Analysis software was used to derive the maximum and minimum jitter value.

PARAMETER MEASUREMENT INFORMATION
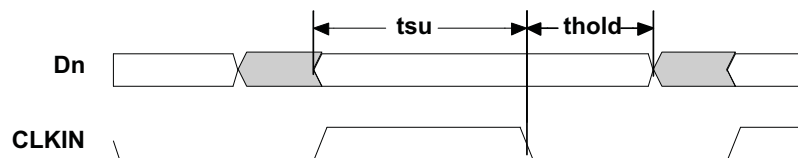
All input timing is defined at IOVDD / 2 on an input signal with a 10% to 90% rise or fall time of less than 3 ns.
CLKSEL = 0V.

Figure 3. Set Up and Hold Time Definition

Product Folder Link(s): SN65LVDS93A

PARAMETER MEASUREMENT INFORMATION (continued)
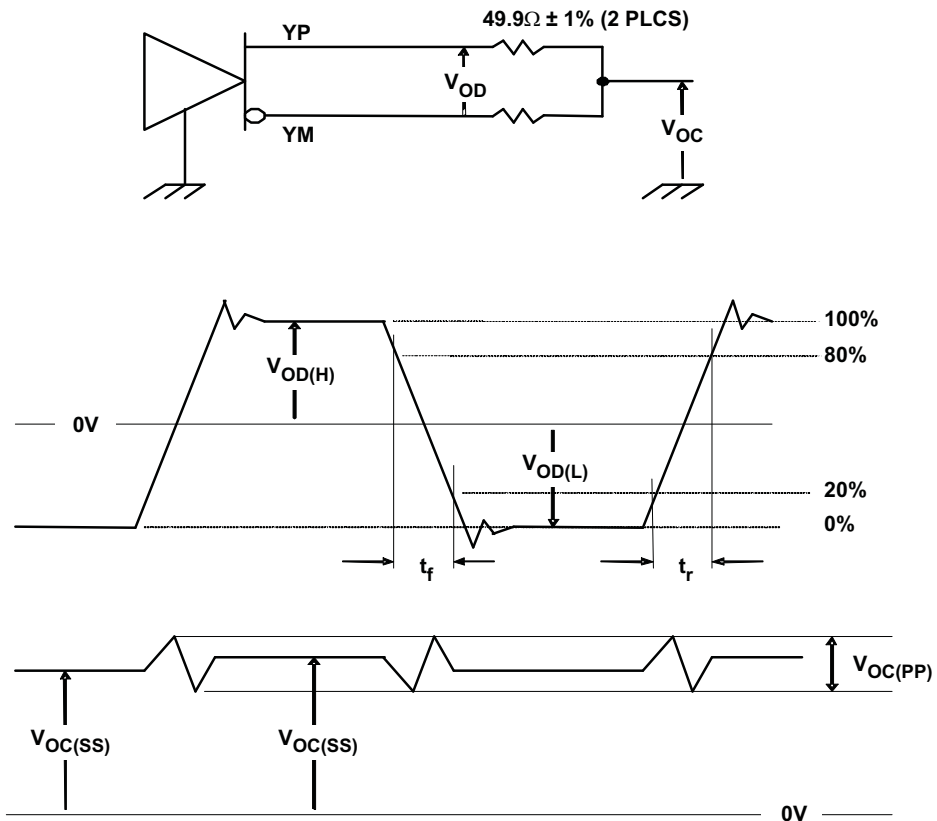
Figure 4. Test Load and Voltage Definitions for LVDS Outputs.
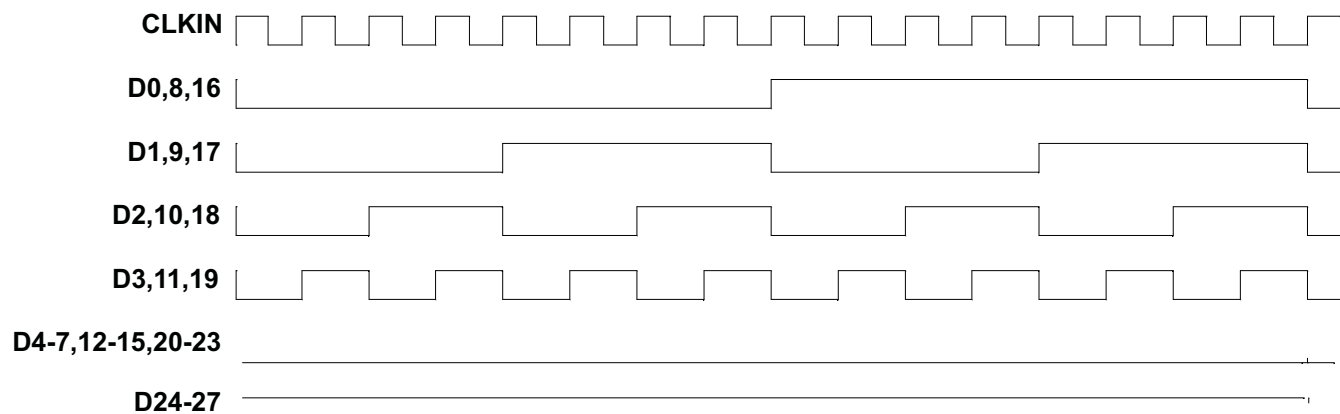
The 16 grayscale test pattern test device power consumption for a typical display pattern.

Figure 5. 16 Grayscale Test Pattern

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PARAMETER MEASUREMENT INFORMATION (continued)
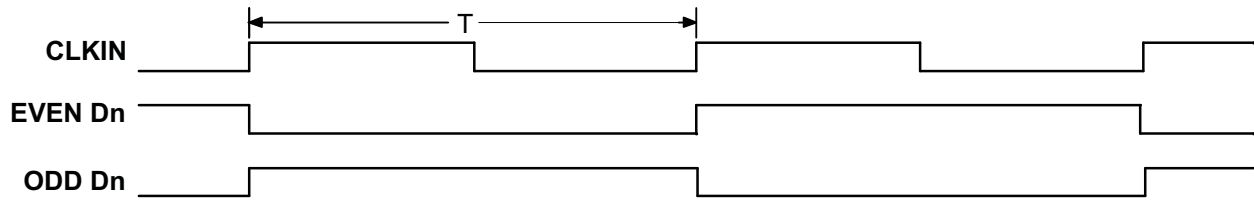
The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs.

Figure 6. Worst-Case Power Test Pattern
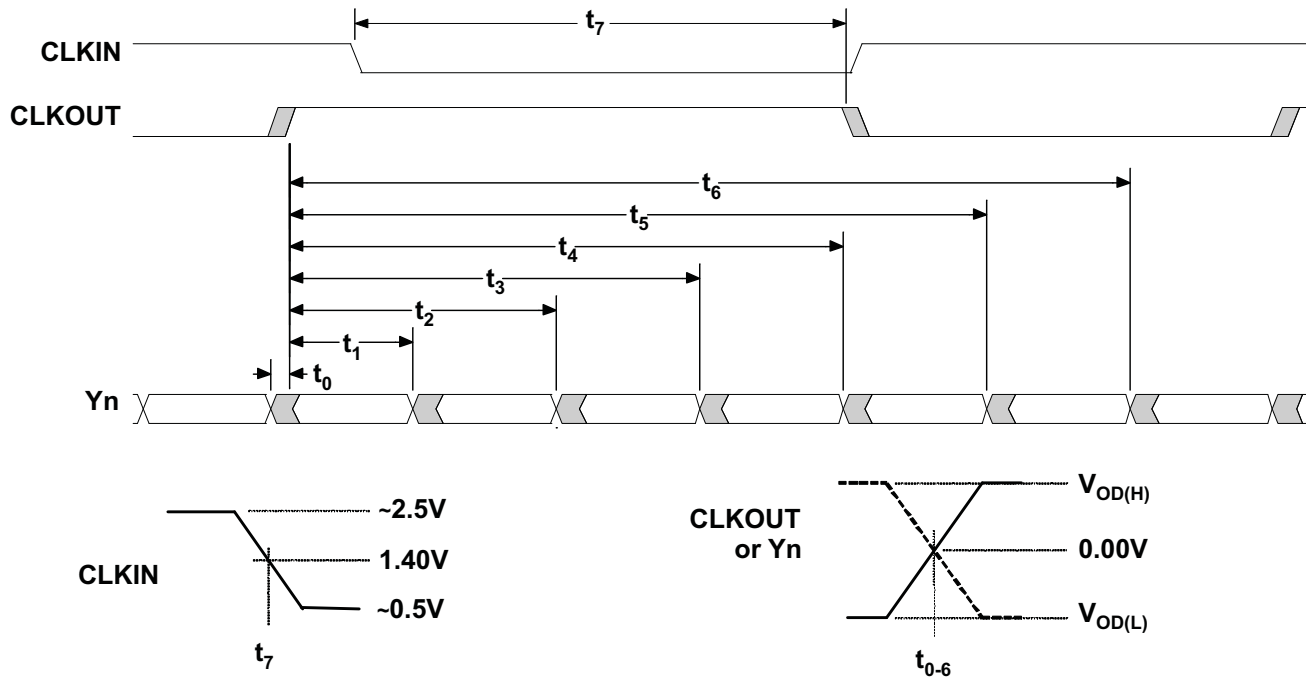
CLKOUT is shown with CLKSEL at high-level.
CLKIN polarity depends on CLKSEL input level.

Figure 7. SN65LVDS93A Timing Definitions

Product Folder Link(s): *SN65LVDS93A*

PARAMETER MEASUREMENT INFORMATION (continued)
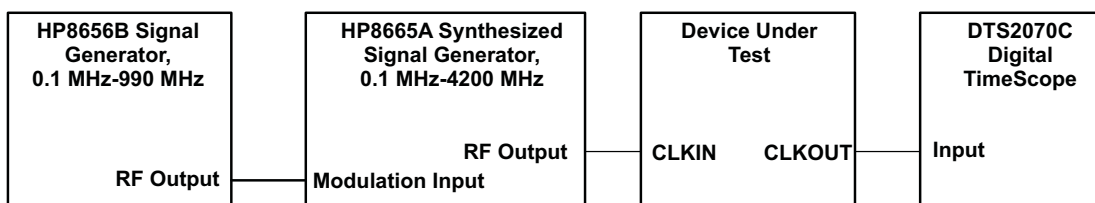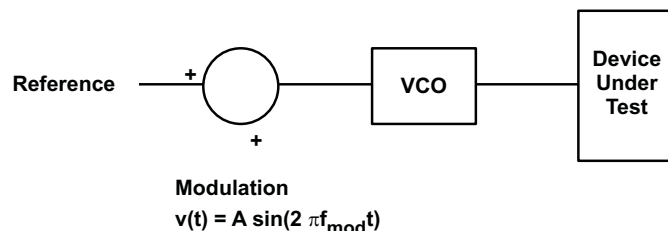
Figure 8. Output Clock Jitter Test Set Up
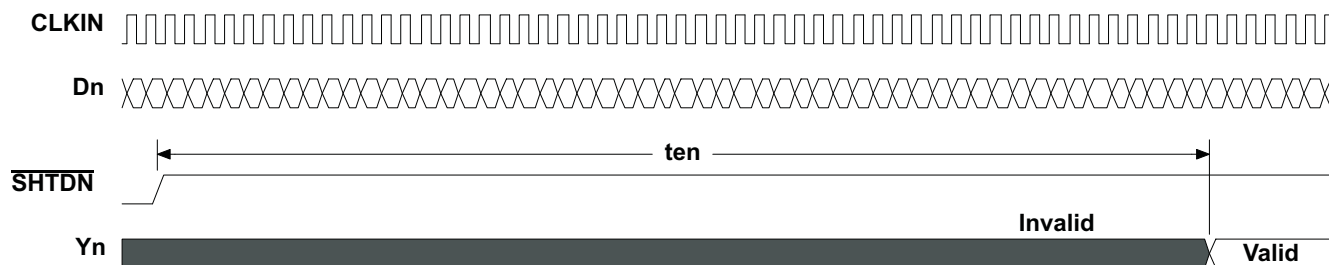
Figure 9. Enable Time Waveforms
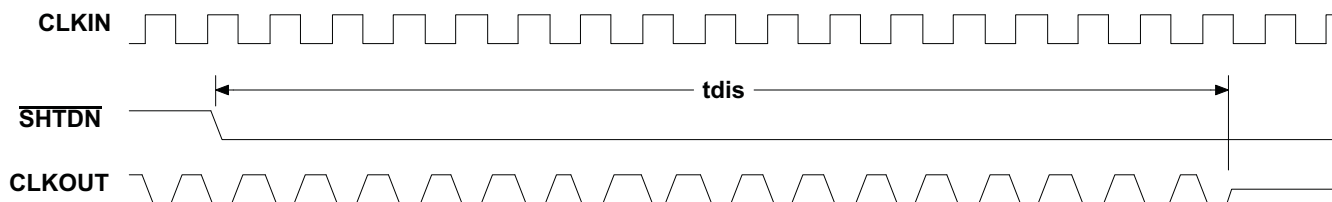
Figure 10. Disable Time Waveforms

Product Folder Link(s): *SN65LVDS93A*

TYPICAL CHARACTERISTICS

AVERAGE GRAYSCALE ICC
vs
CLOCK FREQUENCY

Total Device Current (Using Grayscale pattern) Over Pixel Clock Frequency

$V_{CC} = 3.6V$

$V_{CC} = 3.3V$

$V_{CC} = 3V$

I_{CC} - Average Supply Current - mA

f_{clk} - Clock Frequency - MHz

Figure 11.

OUTPUT CLOCK JITTER
vs
INPUT CLOCK JITTER

Output Jitter

Input Jitter

CLK Frequency During Test = 100MHz

Period Clock Jitter - ps-pp

$f_{(mod)}$ - Input Modular Frequency - MHz

Figure 12.

TYPICAL PRBS OUTPUT SIGNAL
OVER ONE CLOCK PERIOD

CLKL Signal

PRBS Data Signal

Clock Signal: 135MHz

V - Voltage - 80mV/div

t_k - Time - 1ns/div

Figure 13.

Product Folder Link(s): *SN65LVDS93A*

APPLICATION INFORMATION

Power Up Sequence

The SN65LVDS93A does not require a specific power up sequence.

It is permitted to power up IOVCC while VCC, VCCPLL, and VCCLVDS remain powered down and connected to GND. The input level of the $\overline{\text{SHTDN}}$ during this time does not matter as only the input stage is powered up while all other device blocks are still powered down.

It is also permitted to power up all 3.3V power domains while IOVCC is still powered down to GND. The device will not suffer damage. However, in this case, all the I/Os are detected as logic HIGH, regardless of their true input voltage level. Hence, connecting $\overline{\text{SHTDN}}$ to GND will still be interpreted as a logic HIGH; the LVDS output stage will turn on. The power consumption in this condition is significantly higher than standby mode, but still lower than normal mode.

SN65LVDS93A

Typical Application Schematic

Figure 14 represents the schematic drawing of the SN65LVDS93A evaluation module.
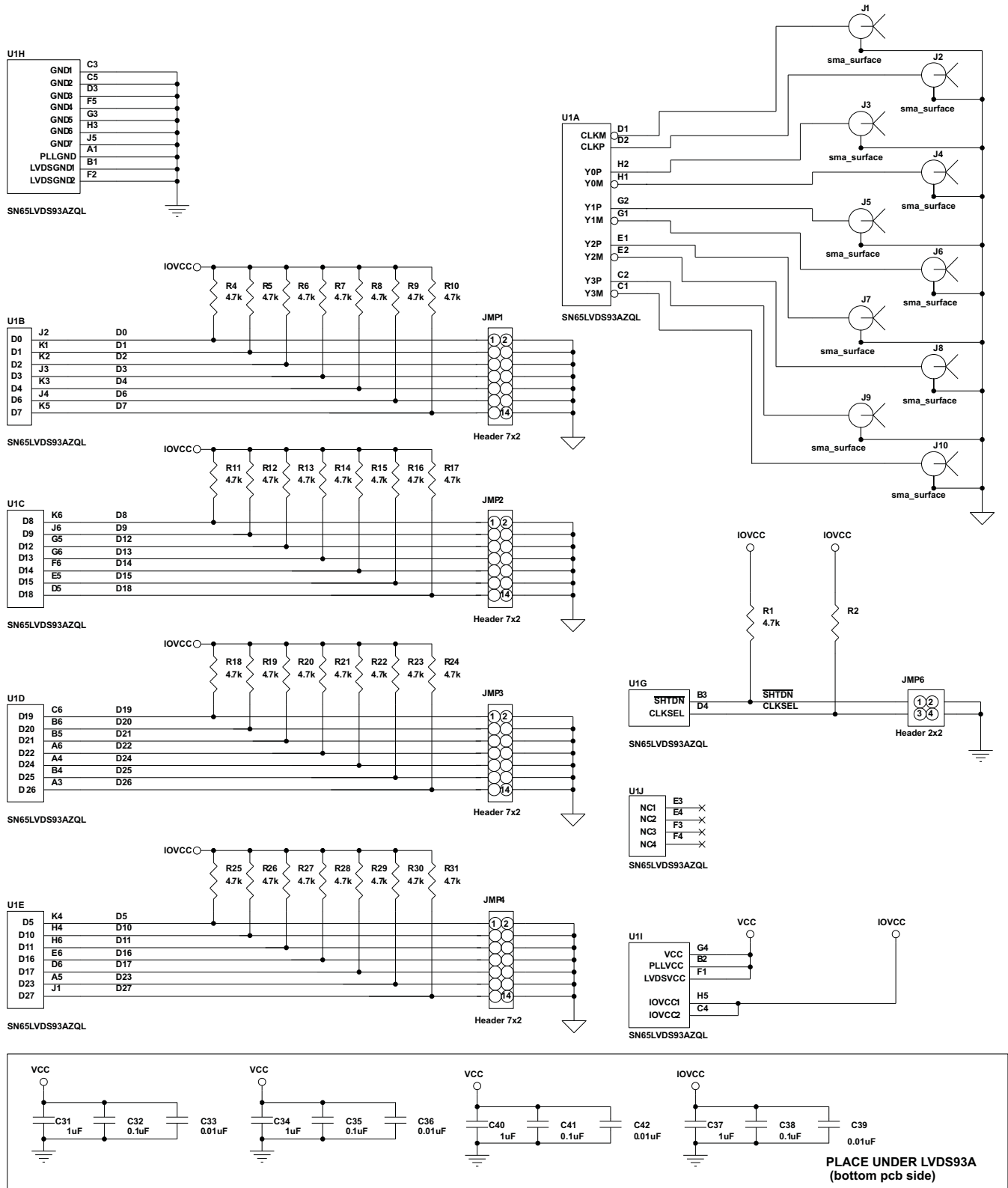
Figure 14. Schematic Example (SN65LVDS93A Evaluation Board)

Product Folder Link(s): *SN65LVDS93A*

PCB Routing

Figure 15 shows a possible breakout of the data input and output signals from the BGA package.
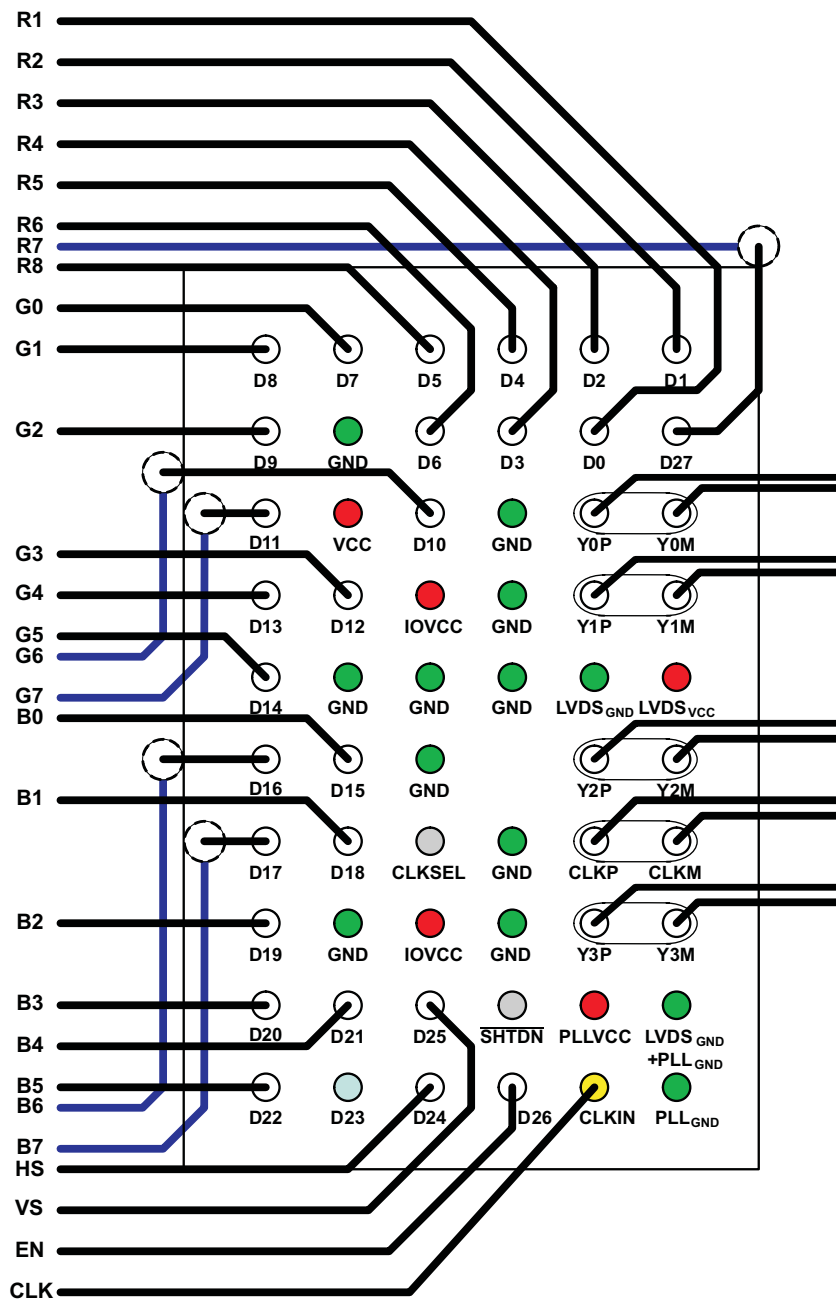
Figure 15. PCB Routing Example

16-BIT BUS EXTENSION

In a 16-bit bus application (Figure 16), TTL data and clock coming from bus transceivers that interface the backplane bus arrive at the Tx parallel inputs of the LVDS serdes transmitter. The clock associated with the bus is also connected to the device. The on-chip PLL synchronizes this clock with the parallel data at the input. The data is then multiplexed into three different line drivers which perform the TTL to LVDS conversion. The clock is also converted to LVDS and presented to a separate driver. This synchronized LVDS data and clock at the receiver, which recovers the LVDS data and clock, performs a conversion back to TTL. Data is then demultiplexed into a parallel format. An on-chip PLL synchronizes the received clock with the parallel data, and then all are presented to the parallel output port of the receiver.
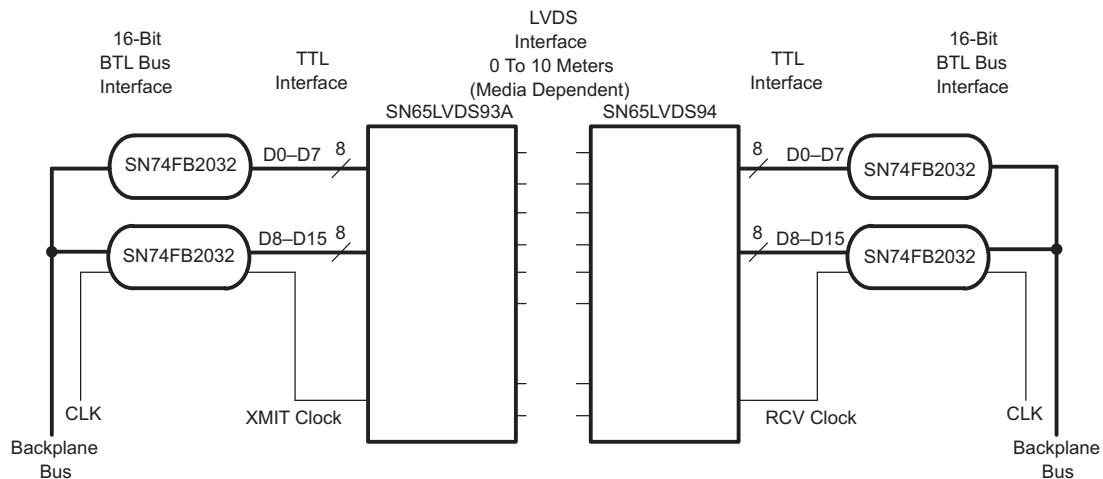
Figure 16. 16-Bit Bus Extension

16-BIT BUS EXTENSION WITH PARITY

In the previous application we did not have a checking bit that would provide assurance that the data crosses the link. If we add a parity bit to the previous example, we would have a diagram similar to the one in Figure 17. The device following the SN74FB2032 is a low-cost parity generator. Each transmit-side transceiver/parity generator takes the LVTTL data from the corresponding transceiver, performs a parity calculation over the byte, and then passes the bits with its calculated parity value on the parallel input of the LVDS serdes transmitter. Again, the on-chip PLL synchronizes this transmit clock with the eighteen parallel bits (16 data + 2 parity) at the input. The synchronized LVDS data/parity and clock arrive at the receiver.

The receiver performs the conversion from LVDS to LVTTL and the transceiver/parity generator performs the parity calculations. These devices compare their corresponding input bytes with the value received on the parity bit. The transceiver/parity generator will assert its parity error output if a mismatch is detected.
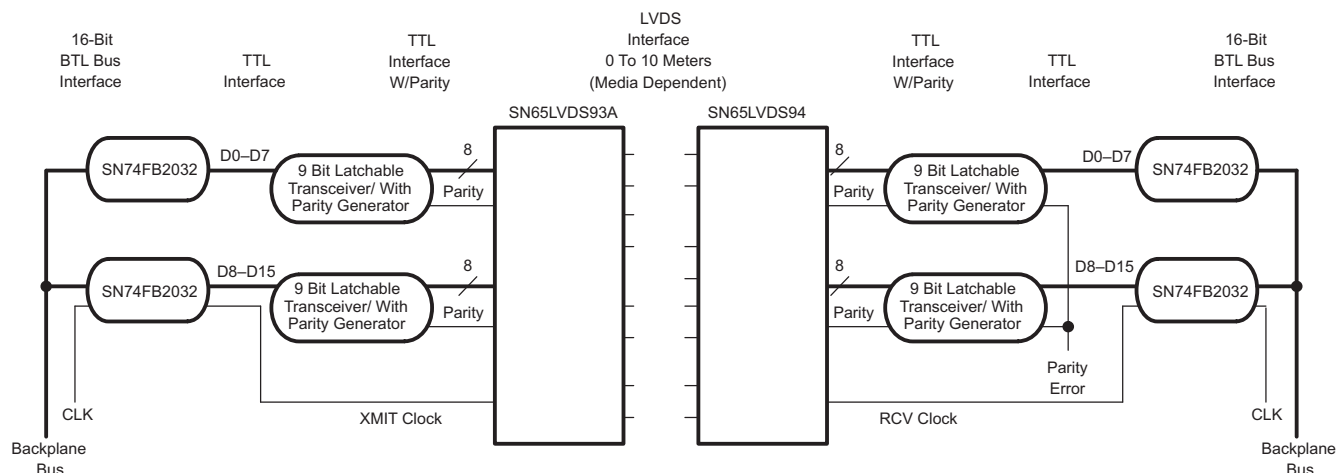
Figure 17. 16-Bit Bus Extension With Parity

LOW COST VIRTUAL BACKPLANE TRANSCEIVER

Figure 18 represents LVDS serdes in an application as a virtual backplane transceiver (VBT). The concept of a VBT can be achieved by implementing individual LVDS serdes chipsets in both directions of subsystem serialized links.

Depending on the application, the designer will face varying choices when implementing a VBT. In addition to the devices shown in Figure 18, functions such as parity and delay lines for control signals could be included. Using additional circuitry, half-duplex or full-duplex operation can be achieved by configuring the clock and control lines properly.

The designer may choose to implement an independent clock oscillator at each end of the link and then use a PLL to synchronize LVDS serdes's parallel I/O to the backplane bus. Resynchronizing FIFOs may also be required.
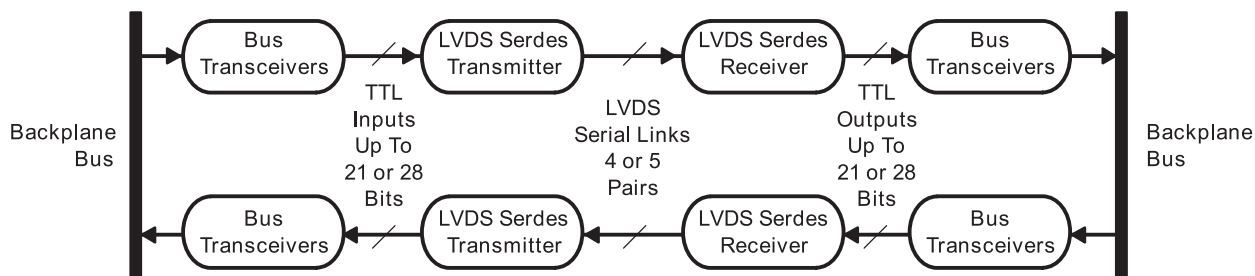
Figure 18. Virtual Backplane Transceiver

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN65LVDS93ADGG	ACTIVE	TSSOP	DGG	56	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDS93ADGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDS93AZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
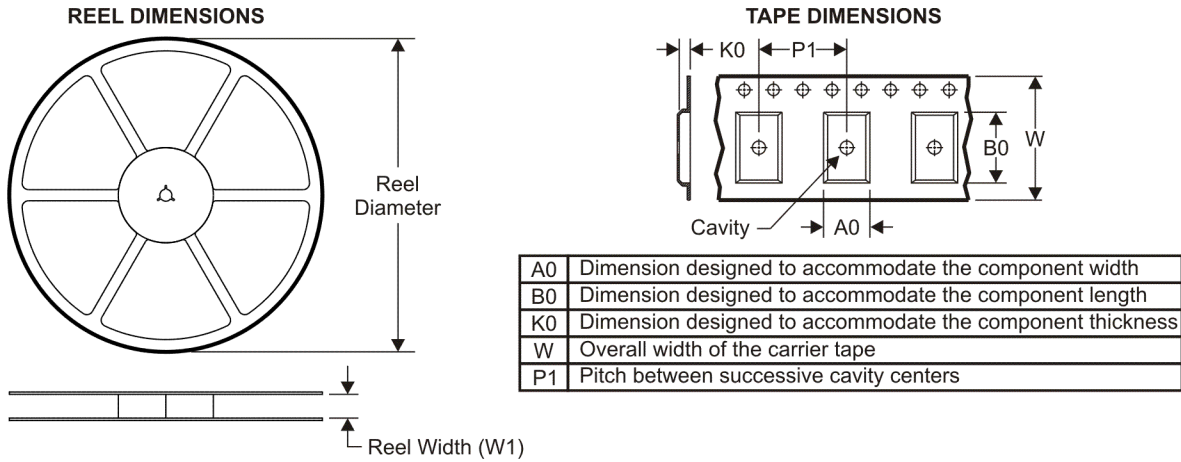
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
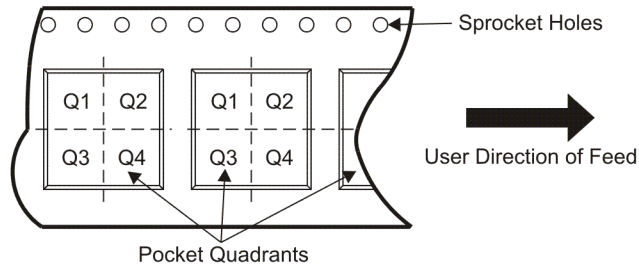
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS93ADGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS93ADGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0

ZQL (R−PBGA−N56) PLASTIC BALL GRID ARRAY

3,25

0,65

0,325

4,60 / 4,40 B

A

7,10 / 6,90

3X Via Hole Without Ball

K J H G F E D C B A

0,65

5,85

0,325

Missing Via Hole Indicates Pin A1 Quadrant

1 2 3 4 5 6

Bottom View

A1 Corner

56X Ø 0,45 / 0,35

| ⊕ | Ø 0,15 Ⓜ C A B |
| | Ø 0,08 Ⓜ C |

1,00 Max

0,10 C

Seating Plane

0,35 / 0,15

C

4204437−3/G 06/2007
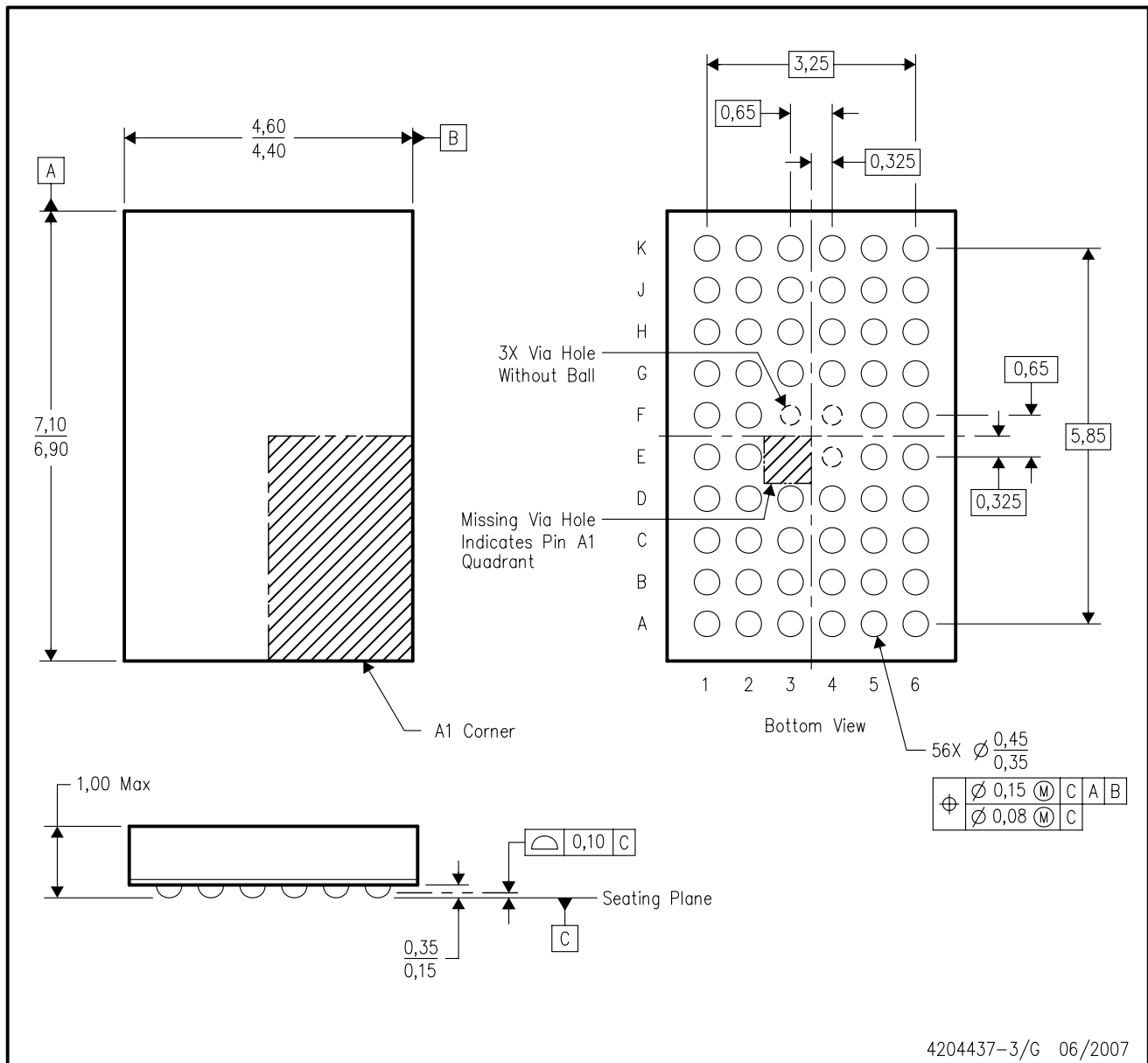
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO−285 variation BA−2.
D. This package is lead−free. Refer to the 56 GQL package (drawing 4200583) for tin−lead (SnPb).

TEXAS INSTRUMENTS
www.ti.com

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

0,50

$\frac{0,27}{0,17}$ ⊕ 0,08 Ⓜ

48

25

$\frac{6,20}{6,00}$ $\frac{8,30}{7,90}$

0,15 NOM

Gage Plane

0°–8°

0,25

0,75
0,50

1

24

A

1,20 MAX

$\frac{0,15}{0,05}$

Seating Plane

△ 0,10

DIM \\ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153